Development of uTCA Hardware for BAM system at FLASH and XFEL

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***Abstract*—This paper describes the design of a uTCA modular card system suited for conversion, sampling and processing of optical pulses. The system consists of a uTCA carrier card along with a double width FPGA Mezzanine Card (FMC) with a changeable optical frontend. The cards were designed for the needs of the BAM system of the FLASH and XFEL accelerators at the DESY facility in Hamburg. The carrier board contains a very powerful FPGA, all required uTCA circuits along with digital interfaces. The FMC card mainly contains four 16-bit fast Analog-to-digital converters (up to 250 MSPS), ADC clock generation and distribution modules, two SFP connectors and a specialized dual RS-485 connection. This paper describes such issues as system organization into universal digital circuits and specialized analog and clock circuits to allow high speed real-time analysis of the properties of thehigh-bandwidth optical signals of the BAM system and better control of the accelerator beam.**

***Index Terms*—BAM, Fast ADC, uTCA, FMC, FLASH, XFEL.**

I. Introduction

The modern superconducting linear accelerator facilities such as the FLASH and XFEL require a very accurate RF field amplitude and phase stability[1]. The field stabilization is assured by the LLRF system and is based on the precision of the field measurement at the frequency of 1.3 GHz [2]. Yet the high requirements are set assuming that the more stable the RF field then the same applies to the accelerator beam. This is not always true, as shown in Figure 1, the beam fluctuations increase with the higher loop gain values due to the amplification of noises. Beam feedback system improves the LLRF control by providing information about the actual beam parameters in real time. With this information, the feedback loop can be closed to maximize the beam stability in addition to the RF field.

To estimate the energy of the electron bunch, the signal from the BAM detector is used to modulate the laser pulses by electro-optical modulator (EOM). These laser pulses are generated with the frequency of 216 MHz. During regular operation in FLASH, bunches are generated with frequency of 1 MHz, which means that every 216-th laser pulse will be modulated, and these modulated pulsed are in the center of out interest (Figure 2).

The height of the modulated laser pulse is proportional to the arrival time. The arrival time is used here as an estimate of the electron bunch energy. It is possible, because depending

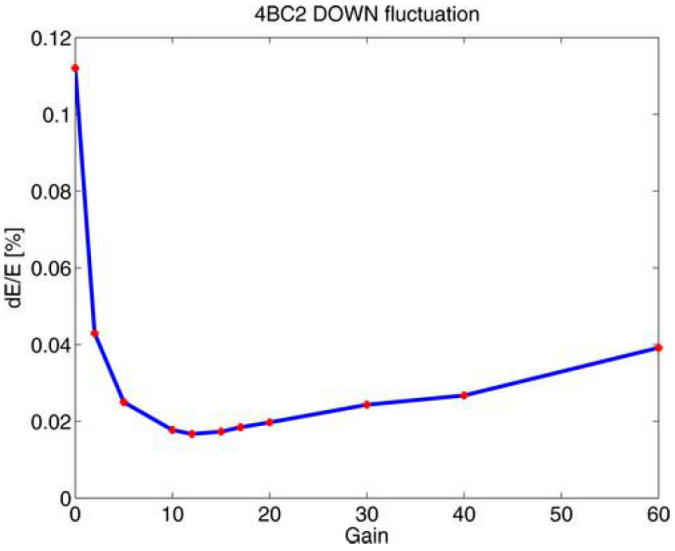

Figure 1. Beam Stability measurement at FLASH

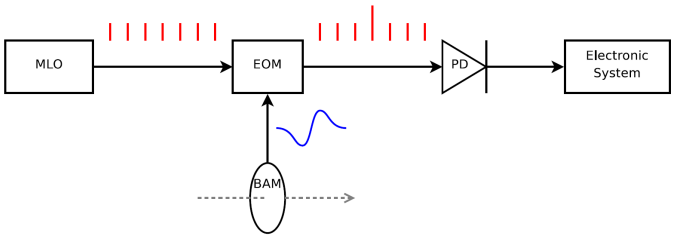

Figure 2. The general concept of the laser pulses modulation

on the energy, electrons travel on different-length ways in the bunch compressor - electrons with higher energy travels using the shorter path, and will arrive earlier, and the electrons with the lower energy, will travel over the longer way, which will result in later arrival. More information about the BAM operation can be found in [3] .

To regulate and minimize the beam fluctuations, proper correction of the RF field amplitude has to be estimated, and applied to the LLRF system. The absolute height of the modulated pulse is not accurate enough, because of the drifts of the signal. Better results are obtained from the relative

height of the pulse. To have the reasonable correction value, relative height of the modulated pulse must me compared with the unmodulated one. The the method of the amplitude correction estimation is show in Figure 3 and equation 1.

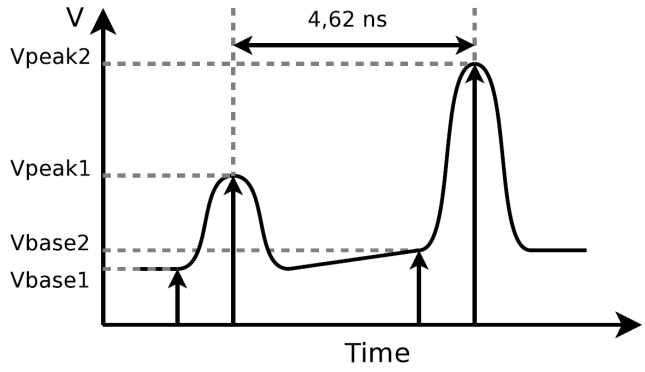

Figure 3. Laser pulses sampling for relative height estimation

$$A_{corr} = \frac{V_{peak2} - V_{base2}}{V_{peak1} - V_{base1}} \quad (1)$$

The VME based system was able to sample laser pulses with maximum frequency of 125MHz, so the only available scheme for sampling was sampling with 108 MHz which means every second pulse. The disadvantage of this method was that incorrect synchronization caused sampling wrong samples, and the modulated samples were not seen. New design based on uTCA with the usage of modern fast FPGAs and ADCs opens the door for introducing much improvement to the system, solving the problem with higher sampling rates without loosing any of the high precision, i.e. by increasing the sampling frequency to the 216 MHz, and then every laser pulse will be sampled.

II. System Conception

The main objective of the project was the design of a two channel optical-signal receiver allowing to sample pulse amplitude. The goal of the system is to obtain from the received optical pulses the information needed for the BAM system. The designed receiver consists of two main modules: a double width uTCA FPGA carrier board and a double width FMC ADC board. An option was foreseen that the receiver can be even used as a stand-alone system with no need for the uTCA crate. The main system conception is illustrated on Figure 4.

Three optical pulsed signals with a repetition rate of 216 MHz and a bandwidth of ~800MHz are fed to the board frontend where they are converted to RF electrical signals. The RF pulses produced must be impedance matched and amplified to reach maximum ADC performance. The front end should also insure very low amplitude and phase noise conversion. One of the resulting signals is used as a reference clock for synchronization of the ADCs. The other two are split to feed four ADCs, i.e. 2 ADCs per channel, to sample the peaks

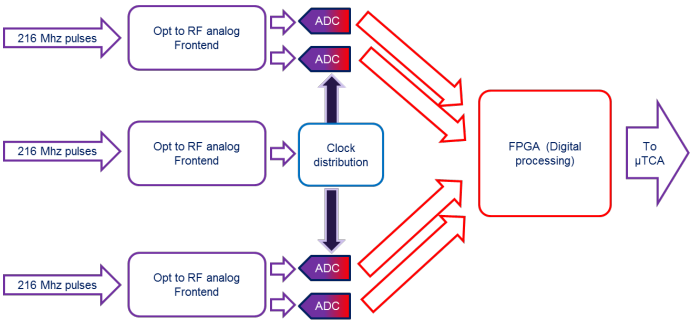

Figure 4. System general conception

and base lines. The data is then sent to an FPGA for signal processing and the calculated information is then passed on to the uTCA synchronization system.

III. System Design and Architecture

In order to achieve proper functioning and desired performance the FMC standard was used and very careful and precise designing techniques were applied to the delicate optical, analog, clocking and even digital circuits of the project.

As stated earlier, the system mainly consists of two boards:

- the uTCA carrier board – containing mainly the digital parts of the system needed for proper acquisition of the data and calculation of the desired correction,
- the FMC ADC board – containing the optical-to-RF conversion, clock distribution, ADCs and specialized communication and control circuits for the BAM system.

The System architecture and layout are shown on Figure 5.

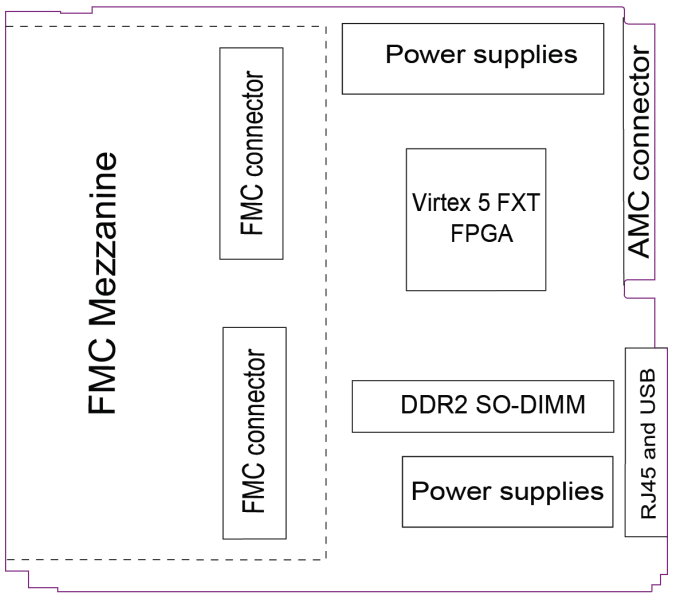

Figure 5. System Architecture and layout

IV. uTCA Carrier Board

The main aim of building this board was to provide a platform, which would be able to host 4 (or in minimal

approach 2) high-speed ADCs up to 1 GSPS, with reserved 16 lines for each device. Additionally, the design fulfills the following requirements:

- Support for a double width FMC;
- AMC.4 compatibility with IPMI support [4];
- High performance FPGA on board;
- Possible operation as a standalone device (full-featured uTCA crate costs 10k Euro).

A. Block Diagram

The block diagram of the carrier board is shown on Figure 6.

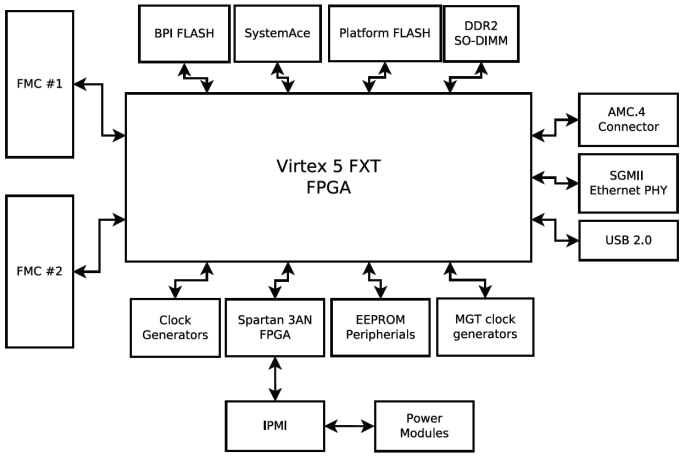

Figure 6. Block diagram of carrier board

B. Main Features

The main features of the carrier board are:

- Two single or one double size FMC mezzanine support;
- Over 70 differential pairs or 140 single ended signals available for each FMC slot;
- Four gigabit serial channels per FMC slot;
- Virtex5 FXT70 FPGA with embedded PowerPC440 processor;
- DDR2 SO-DIMM connector;
- IPMI unit;
- Advanced configuration modes with fail-safe configuration memory;
- CF card as a configuration memory, and non-volatile storage for embedded systems;
- Serial port and JTAG over USB;
- Gigabit Ethernet PHY and RJ45 socket for stand-alone operation;
- Low noise power supply modules;
- Watchdog and configuration supervisor implemented in separate small FPGA;
- AMC.4 communication lanes:
  - Gigabit Ethernet;
  - PCI Express;
  - Two point-2-point links;
  - Two M-LVDS links;
  - CLKA and CLKB routed to FPGA;
  - JTAG.

The assembled board is shown on Figure 7.

V. FMC ADC BOARD

The ADC board is a double width FPGA Mezzanine Card (FMC)[5] which is specialized for the FLASH and XFEL BAM system. It consists of the optical-to-RF conversion circuits, clock generation circuits, ADCs, a specialized dual RS-485 connection, and communication ports.

A. Block Diagram

The block diagram of the FMC ADC board is shown on Figure 8.

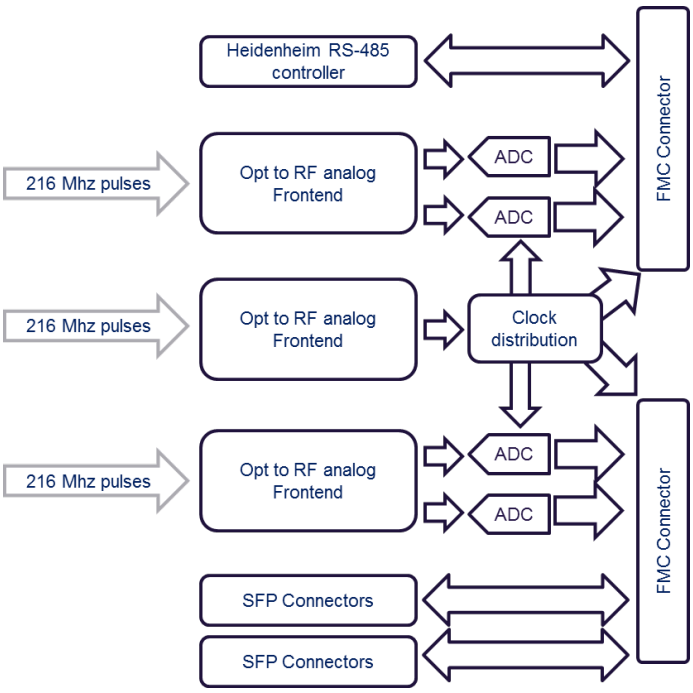

Figure 8. Block diagram of FMC card

B. Main Features

The circuits of the FMC board can be divided into three main groups:

1) The pulse sampling circuits: The pulse sampling circuits consist of an optical-to-RF conversion scheme using a photodiode and a transimpedance amplifier. This part is designed as a piggyback allowing the switching between different photodiodes and transimpedance amplifiers. This procedure increases the modularity of the system and allows choosing the best parts according to bandwidth, lowest noise, distortion and matching.[1] The obtained RF signals are then split into two channels and afterwards amplified, differentiated and matched to the input of the ADCs using a very low noise and distortion

[1]The piggyback has an additional feature to use the designed hardware for purposes different than the BAM system where high precision fast sampling of analog signals is needed.

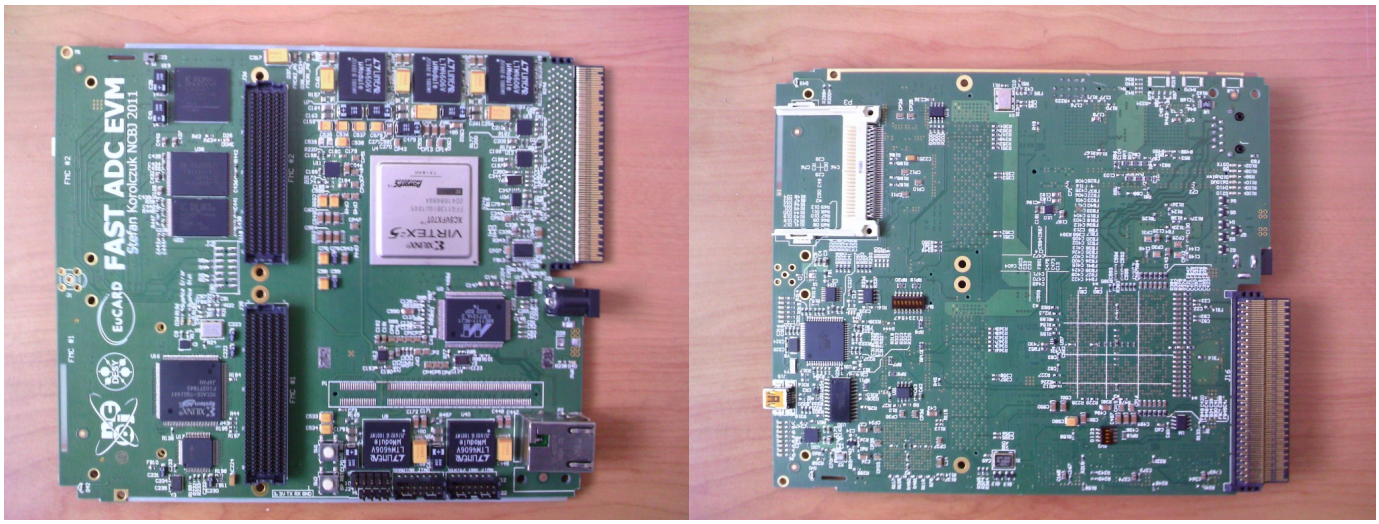

Figure 7. Assembled uTCA carrier board

amplifier with very low phase and amplitude imbalance to maximize ADC performance. The differential signals are then sampled with 16-bit fast analog-to-digital converters at a sampling rate of 216 MSPS (same as incoming pulses). Each channel consists of two ADCs for sampling the peak and baseline of the incoming pulse.

The same optical-to-RF conversion is used for the reference pulses that are used to synchronize and clock the ADCs. The two split channels are fed into a low jitter PLL chip that uses one input for clock distribution and the other as reference for the built-in PLL. The choice of operation is set by the FPGA on the carrier board. There are two clocks from the chip connected to each ADC. One is a phase-tunable low noise LVDS clock and the other an even lower noise LVPECL clock which additionally has the possibility to install fixed delays on the lines. The generated clock signals are also sent to the carrier board to insure synchronized data acquisition and processing. The programmable and fixed delays are inevitable to set the sampling points to exact time values, i.e. to sample the peak and baseline of the incoming pulses.

2) The Heidenheim controller circuits: The controller is a specialized communication port used in the BAM system. It consists of two Half-duplex RS-485 transceivers. One is used for sending the clock to the Heidenheim controller, while the other for sending and receiving data form it.

3) SFP communication ports: The board has two SFP connector added to allow fast two-way optical communication with the rest of the uTCA systems.

C. PCB Design

The design of the FMC board had to be strictly prepared according to the rules of signal integrity and RF analog design to insure low noise, low jitter, and low distortion high precision ADC, clocking, and digital circuits [6]. The designed FMC board is shown in 9.

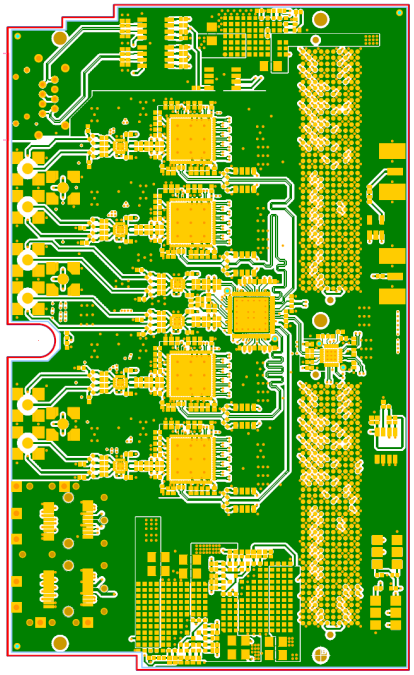

Figure 9. FMC PCB design

VI. Measurements

To insure the feasibility of the designed modules, some tests and measurements were prepared and made in the specialized laboratory.

A. Front-end Measurements

The front-end consisting of the photodiode, optical-to RF conversion and power splitting and amplification was measured using laser pulses identical to the ones in the FLASH accelerator (and XFEL in the future). The pulses were analyzed with a very fast oscilloscope and a signal source analyzer to insure proper functioning and low amplitude and phase noise.

Example differential pulses from the measurement are shown in Figure 10.

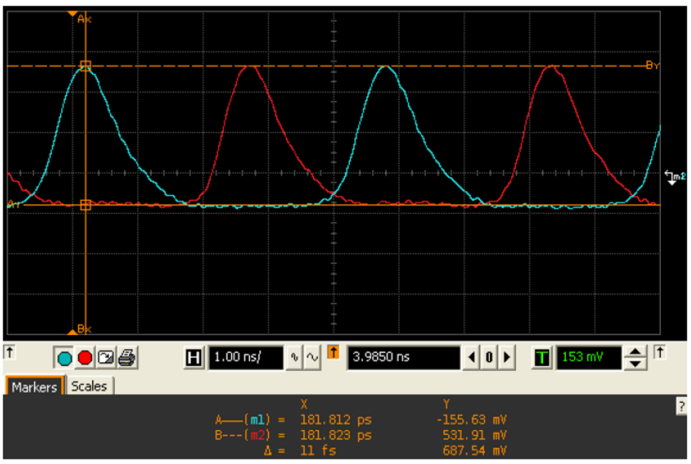

Figure 10. Front-end pulses after conversion and amplification

The measured phase noise of the pulses after conversion was around 170 fs integrated over a bandwidth from 10Hz to 1MHz.

B. ADC Measurements

The designed front-end was connected to the used ADC evaluation board to measure precision and feasibility of the design. Two signals were used: one as an input and the other for clocking the ADC through a chip for tuning the phase. 16K samples were made at every time point and the averages were use to prepare the plot shown on Figure 11.

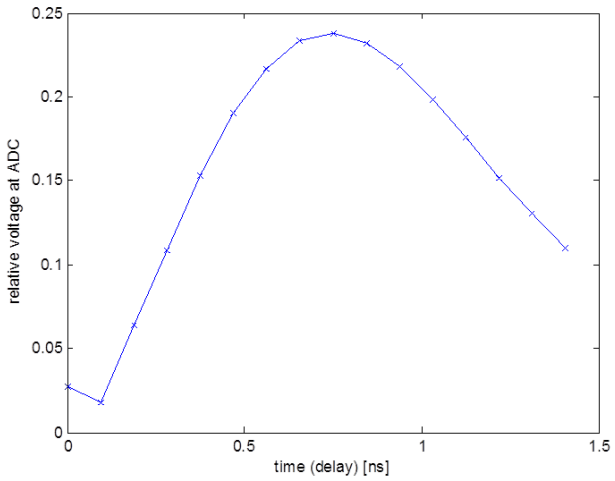

Figure 11. Sampled converted optical pulse

The measurements showed a sampling instability of below 0.19%. To insure even better precision in the designed system a different differential amplifier was used with much better characteristics in terms of noise and distortion. The clocking circuits on the FMC board are also prepared to be of lower jitter. Moreover, the clock and analog circuits are better matched at the given frequencies to obtain the best possible performance.

VII. Summary

A set of boards was prepared for the BAM system for the FLASH and XFEL accelerators. It consists of a universal uTCA carrier board containing a powerful FPGA and digital circuits along with a specialized FMC board with high precision fast ADCs that converts and samples the optical signals used in the BAM system. The designed circuits were tested for feasibility with signals identical to the ones in the accelerator. Moreover the designed modules can be used as a stand-alone system to allow fast sampling, processing and analysis with very high precision of various optical and RF signals.

Acknowledgment

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