Chapter 4

Data Acquisition and Detector Control

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This chapter provides an overview of NA60's data acquisition system and the work leading to successful data taking. We will cover the NA60 DAQ architecture, the use of personal computers in readout applications and the PCI readout cards developed for NA60. Since much of the work developed has been published in some form, details can be obtained from Appendix B, which includes integral versions of publications where I am one of the main authors.

The readout architecture of NA60 [1] can be roughly divided into two main areas: hardware and software. Hardware is closer to the detector's front-end electronics, where the jargon includes objects and concepts like FPGA, VHDL, PCI or interrupt servicing. Software is closer to permanent data storage, and includes keywords like bandwidth, parallel processing and network thoroughput. Wherever the border between these two "worlds" is, this chapter crosses it, reflecting the broadness of the work developed.

We finish with an overview of the detector control system of NA60.

4.1 Data Acquisition System: DAQ

This section overviews the main software and hardware components in the DAQ of NA60. Further details on the DAQ architecture of NA60 can be found in appendix (section B.1, on page 141).

4.1.1 Software

On the software side, NA60 built its DAQ system around the Data Acquisition and Test Environment (DATE) [2] developed for the ALICE experiment at CERN.

Event building

DATE's foremost function is to gather an event's data from each sub-detector and build a full event from many sub-detectors. For that, the concepts of Local Data Collector (LDC) and Global Data Concentrator (GDC) are crucial. Each LDC is responsible for the readout of a sub-detector or fraction thereof: e.g., while the muon spectrometer was read out by one LDC, the pixel tracker needed up to six LDCs. Furthermore, NA60 used LDCs to save important information integrated in scalers during the SPS spill, like the integrated beam intensity or the ACM magnet current. Each LDC can comprise several readout "partitions": for instance, each LDC for the pixel tracker serviced more than one plane.

Finally, depending on the required data thoroughput, one or several GDCs are scheduled in a round-robin fashion to join the sub-event pieces together into a full event. These events are cached locally in each GDC and subsequently shipped to CERN's Central Data Recording (CDR) facility over a dedicated high-speed link.

Run Control

This function is responsible for keeping all LDC and GDC elements synchronised: e.g., each and every LDC needs to know where to ship its data for the next event.

It is also this part of DATE that starts and ends runs and keeps statistics on the amount of data generated by each LDC, recorded by the GDCs and the status of the memory buffers in between those steps.

Monitoring

Profiting from the networked nature of the LDC to GDC transfers, DATE not only handles event assembly but also provides a monitoring framework. It is clear that monitoring of detector response and performance is very important in guaranteeing the quality of the data being recorded. It was shown to be much more convenient to monitor the data online, instead of waiting for a run to be over and only then checking what had happened. Thanks to DATE, these two possibilities were transparent to the monitoring software: you can either subscribe to the monitoring stream of an LDC or to a GDC raw data file.

DATE customisations

During the lifetime of NA60, a large number of modifications and improvements were done to the original DATE package. The main ones are described below.

Beam spill characteristics The most important modification was to adapt the collider nature of DATE (developed for ALICE at the LHC) to the fixed-target nature of NA60 (operating at the SPS).

Collider experiments usually have readout systems that continuously push data forward, since their beams collide for many hours between ring fills. Fixed-target experiments, on the other hand, operate at very different duty cycles; the SPS, depending on the particles being accelerated and on their energy, provides a uniform spill of beam particles for 2–5 s every 15–20 s. This leads to the fact that, traditionally, fixed-target experiments buffer all the data produced during the beam spill, and then profit from the time between spills to read it out of the detectors and into permanent storage.

Clearly this only works if the amount of data is small compared to the memory technology available, or if the time between spills is long enough.

The solution found for NA60 introduced an intermediate layer that, at every end of spill, parses the data from the detectors and slices it into events, which are buffered in large shared memory segments. DATE then takes the data from these buffers and proceeds normally, as if data would be produced "continuously".

Low-level interfacing Another aspect fully developed by NA60 are the low-level software interfaces to the electronics. This included "gluing" many standard technologies like GPIB or VME to

DATE. But the most laborous task was to develop the interfaces to our own PCI electronics. Interfacing and reading them out was rendered much easier for DATE using a device driver which presented the PCI card's memory to the DATE readout process as a plain memory area.

4.1.2 Hardware

On the hardware side, NA60 has heavily relied on personal computer (PC) technology to implement all of its different data acquisition systems in 2002, 2003 and 2004. In fact, every detector system has been interfaced to the DAQ using one or more PCs. Furthermore, new systems like the silicon pixel tracker or the microstrip tracker do not include any conventional readout electronics used in high-energy physics, like CAMAC, VME, FastBus, etc.

Why new hardware?

The muon spectrometer readout is based on the Readout Memory Hybrid (RMH) technology developed at CERN more than 30 years ago. Its principles are adequate to the readout of wire chambers; when the system is triggered for readout, each hit present in the detector generates an encoded word providing the location of the hit. An event's data is thus a list of encoded hits that funnel down through two layers of encoders (crate encoders and system encoder). This information ends up in a memory buffer which is read out between SPS spills.

For NA60 it was clear that, after upgrading the DAQ system such that the pixel tracker would not limit the number of events acquired per spill, the muon spectrometer readout memory would then be the bottleneck, imposing a severe toll on the number of dimuon triggers recorded per SPS spill.

The solution came in the form of PCI cards that could work as general-purpose carriers to mezzanines specific for each detector. The generic part provides event formatting and buffer space for data storage during the spill duration, while the mezzanine would interface the front-end electronics, both physically, electrically, and in terms of data format.

PCI readout

In the beginning of 2001, the CERN Electronics Group of the Experimental Physics division (EP-ED) was starting the development of a PCI readout card that would allow fast readout to a large memory buffer inside a PC. This card was christened Flexible I/O Card (FLIC) [3]. In parallel, studies on the feasibility of using the PCI bus bandwidth were started. Results showed that this bus was adequate for the readout needs of NA60 [4]. With time, and after the first run of NA60 in 2002, the FLIC design showed several shortcomings. This lead to the design of a new card: the PCI Compact and Flexible Design (CFD) [5].

PCI reading with a PC NA60 chose to base the whole of its readout scheme around personal computers equipped with PCI readout cards. The PCI standard [6] includes 32 and 64-bit wide buses operating at 33 or 66 MHz. The maximum theoretical bandwidth provided by the 32-bit 33 MHz PCI bus found in every personal computer is 132 MB/s and was thought adequate for NA60's readout needs.

In order to ensure that this was a viable solution for the NA60 detector readout, a battery of tests was performed in reading many different kinds of PCI cards with many PC mainboards. First tests gave very disappointing results of only a few MB/s. As the understanding of the interaction between the computer's CPU and the devices in the PCI bus grew, read speed values steadily increased, until a breakthrough occurred, whereby a read speed of 36 MiB/s was achieved. Though this is about 30% of the theoretical maximum, we need to take into account that these are read operations, intrinsically slower than write operations. Furthermore, the ability to sustain a (bursted) PCI transaction in CPU initiated reads is very limited, which led to a unique choice of PC hardware, the ASUS-A7M mainboard.

Notwithstanding, the results obtained were good enough to demonstrate that PC technology was able to provide the needed bandwidth, using readily available (low-cost) personal computer systems. Curiously, the manufacturer of the components in the final hardware choice that provided such high speeds could not explain the performance of its system.

Further details on PCI reading can be found in appendix (section B.2, on page 151).

The PCI-FLIC The PCI-FLIC was built around the ORCA PCI FPSC as the programmable element. There is a 64 MiB SDRAM buffer and a PCI-to-PCI bridge that isolates the PCI bus inside the FLIC from the external world. The FLIC provides PCI connectivity to its mezzanine connector, a feature intended for use with PMC compatible mezzanines like the TTC-Rx used in first read tests, when the ORCA SDRAM controller was not yet available.

The FLIC is compatible with both 32 and 64-bit PCI buses. While the ORCA FPSC would allow for operation in 66 MHz PCI buses, we have seen that performance would be limited by even the any more complex logic (like the SDRAM controller) in the FPGA part.

The ORCA FPSC comprises an ASIC PCI core along with programmable FPGA logic. The amount of FPGA logic is quite limited, besides the fact that the manufacturer optimised the ORCA cell-blocks, routing and layout tools for switching fabric, used in high-speed telecommunications applications. As a consequence, our SDRAM memory controller as implemented in the ORCA could never be clocked faster than 10 MHz.

Further information on the FLIC can be found in appendix (section B.3, on page 185).

The PCI-CFD While the FLIC performance was enough to read out the muon spectrometer RMH system, as well as to test a few ALICE pixel planes (that work at 10 MHz), it was soon realised that a much more performant approach to using PCI would be required to read the full pixel tracker.

From that need, the CFD was born. It replaces the ORCA FPSC by a large Altera FPGA in tandem with the PLX PCI 9030 ASIC PCI adapter. This allowed for much more space in the programmable part of the FPGA (the whole device was now programmable), while the PLX bridge would take care of interfacing the PCI bus. Moreover, Altera's technology is adapted to general-purpose firmware synthesis, which easily allowed the SDRAM controller to be clocked at 40 MHz. The CFD also removes the PCI bridge, making the mezzanine expansion not PMC compatible, but rather completely custom. This allowed for a much simpler board design and increased connectivity to the mezzanine by using pins otherwise reserved to PCI routing in the FLIC card. Finally, the CFD includes a unique identifier, which proved very useful in identifying which detector slice was connected to which piece of data.

The CFD was used for the readout of the zero degree calorimeter, pixel tracker and beam tracker in NA60, besides other applications external to NA60. Other solutions were used for the muon spectrometer (which could be appropriately read out by the FLIC) and the microstrip tracker, whose readout is discussed in detail in subsection 3.2.3 on page 35.

Further details on the CFD card can be found in appendix (section B.4, on page 191).

4.2 Detector Control System: DCS

The NA60 Detector Control System (DCS) provides control and monitoring of the cooling and gas systems, through PLCs, and of the power supplies and high voltages, through CAENET and CAEN OPC servers. The PVSS and BridgeVIEW software packages centralise, archive and display the DCS data. Two Windows 2000 PCs in the control room provide the user interface for the shift-takers.

Fifteen CAEN SY403 crates located in the control room provide the high voltages needed for the photo-tubes of the trigger hodoscopes, ZDC and quartz blade, and interaction counter. In the beam area, two SY1527 CAEN crates provide the high and low voltages needed by the silicon detectors (the beam tracker, the silicon microstrip tracker and the silicon pixel tracker) to bias the sensors and power the electronics. These crates are interfaced with the high-level software through CAEN OPC servers, either via CAENET (SY403) or Ethernet (SY1527).

A Wago PLC is used for the automatic regulation of the cryogenic system of the beam tracker, depending on the temperatures measured on the detectors, using Pt100 Wago modules. The same devices provide temperature monitoring for the microstrip and pixel trackers. A Schneider PLC controls the gas flow and mixture in the muon tracking chambers. It is interfaced with PVSS and Bridgeview through a Schneider OPC Server running on a Windows PC. In case of need, the DAQ PCs located in the beam area can be reset from the counting room using the PVSS user interface to command interlock relays, through the Wago system.

The top-level SCADA application was developed using PVSS software, communicating with the hardware via the OPC servers. PVSS panels were developed for all the equipments using the JCOP framework, developed by the CERN IT/CO group. A main panel shows the most important parameters of the experiment, and gives access to more detailed views of specific sub-systems in specific panels. The time evolution of the most important DCS values is permanently on display using a Bridgeview application. These values are also regularly exported to an external archiving system, based on MySQL, and can be consulted from any web browser through a CGI Perl script. Such history browsing are very useful during the online and offline data analysis.

In general, we can say that our PVSS-based Detector Control System worked quite smoothly in the 2003 indium run, with less problems than during the June 2002 proton run. Several pragmatical solutions were implemented (resets, automatic restarts, fully devoted PCs, etc) to minimise the frequency and importance of the problems.

Bibliography

[1] M. Floris, D. Marras, G. Usai, A. David, P. Rosinsky, and H. Ohnishi. The NA60 experiment readout architecture. *IEEE Trans. Nucl. Sci.*, 51(3):430–438, June 2004. DOI 10.1109/TNS.2004.828828. 41

[2] CERN ALICE DAQ group. *ALICE DATE User's Guide*, January 2001. ALICE 00/31 Internal Note/DAQ. 41

[3] J. Toledo, H. Muller, J. Buytaert, F. Bal, A. David, A. Guirão, and F.J. Mora. A plug and play approach to data acquisition. *IEEE Trans. Nucl. Sci.*, 49(3):1190–1194, June 2002. DOI 10.1109/TNS.2002.1039635. 43

[4] André David. *Performance issues in PCI reading*, 2001. NA60 Note 2001-3. 43

[5] M. Floris, C. Cicalò, D. Marras, G. Usai, and A. David. A new PCI card for readout in high energy physics experiments. *IEEE Trans. Nucl. Sci.*, 51(5):2086–2090, October 2004. DOI 10.1109/TNS.2004.835567. 43

[6] D. Anderson and T. Shanley. *PCI System Architecture*. Addison-Wesley, 4th edition, January 1999. ISBN 0201309742. 43