1 The Minivertex Detector (VDET)

Description VDET I (1991 - Oct.1995): Two concentric layers of silicon wafers, at radii of 6.3 and 10.8 cm are placed around the beam pipe. The silicon wafers have readout strips on both sides: strips oriented parallel to the beam ("$r-\phi$ side") measure the ϕ-coordinate of particle tracks whereas the z-coordinate is measured by strips perpendicular to the beam on the other side ("z side").

The distance between strips, called pitch, is $25\mu m$ on both sides. The readout pitch is $100\mu m$. On the z side, every other strip serves as a "blocking strip", collecting no ionization charges; thus the effective strip pitch on the z side is $50\mu m$. Capacitive charge division is used to interpolate the track impact point between readout strips using a centre-of-gravity method. The CAMEX64 amplifier chips (64 channels each with a pitch of $100\mu m$) are bonded directly to the strips and mounted at the ends of the detector for the readout of the $r-\phi$ side. The amplifier chips for the z- readout are mounted above the silicon detectors.

Dimensions:	Inner layer:	R $\approx$ 6.3 cm	length $\approx$ 20.0 cm
	Outer layer:	R $\approx$ 10.8 cm	length $\approx$ 20.0 cm
	Total thickness:	0.041 X_0 at $\theta = 90^0$	averaged over ϕ
	Silicon detector wafers:	thickness	$\approx 300\mu m$
		size	$5.12cm \times 5.12cm$

Readout: Analogue readout

Each module has 512 strips read out on the rϕ-side and 1024 strips read out on the z-side. Every 256 strips are multiplexed onto 1 "line". This leads to 2 output lines for the z-strips and to four output lines for the rϕ strips per module. In total this gives 6 lines/module $\times$ 9 (15) modules/side $\times$ 2 sides = 108 (180) signal output lines for the inner (outer) layer. Thus the 73728 strips are output with 288 analog lines.

1991 and 1992 Performances: Signal-to-noise ratio: 14:1

Point resolution: $\sigma_{r\phi} \approx 12\ \mu m$, $\sigma_z \approx 10\ \mu m$ for normally incident tracks

Description VDET for LEP II: A new silicon vertex detector (VDET II) was developed during 1994-1995 to replace the former detector for the high energy running periods of LEP after October 1995. The main reason for the upgrade was to increase the discovery potential for the Higgs search by extending the angular coverage of the detector and by reducing the material in the tracking volume. In addition the sensitivity to radiation was reduced to cope with the expected higher radiation level at LEP II. The design and the performance is described in the following in more detail.

The physical strip pitch is the same as for the present detector. The pitch of readout strips is reduced by a factor of two for the $r\phi$ side (now $50\mu m$) and identical to the previous design for the z side. To connect the 1920 readout strips per module on the z-side with the 1024 electronics channels at the end of the detector, the strip-pairs

(1,961), (2,962) ...(960,1920) are multiplexed onto the same electronics channel each, using a thin microstrip kapton layer bonded to the z-readout strips. The MX-7RH amplifier chip used is specially processed and can stand a radiation dose of up to 1 Mrad. It has 128 channels, low noise and eight chips are bonded to the readout strips per side.

The new detector improves the performance of Aleph as follows:

- it uses six silicon wafers per face with a length of 6.5 cm each, thus doubling the active length compared to the former detector. This increases the angular acceptance to $-0.95 < cos\theta < 0.95$ for tracks required to hit at least one layer,
- to cope with the higher level of radiation expected at LEP II less radiation sensitive electronics is used (max. dose of 1 Mrad),
- to reduce the amount of passive material the readout electronics previously mounted across the sensitive region above the silicon wafers on the z-side is now mounted at the far end of the detetor. This decreases the tails in the track-impact parameter resolution and improves b-tagging.

The internal allignment is facilitated by larger regions where wafers overlap, thus increasing the statistics of tracks to be used for the allignment.

Dimensions:			
	Inner layer:	R = $\approx$ 6.3 cm	length $\approx$ 40.0 cm
	Outer layer:	R = $\approx$ 11.0 cm	length $\approx$ 40.0 cm
	Total thickness:	0.015 X_0 at $\theta = 90^0$	averaged over ϕ
	Silicon detector wafers:	thickness	$\approx 300\mu m$
		size	$5.26cm \times 6.54cm$

Readout: Analogue readout

Each module has 1024 strips read out for both the rϕ and the z-side. All 1024 electronic channels per module/side are multiplexed onto one "line". The total of 95088 strips are thus output onto 48 analog lines, further amplified ... and finally digitized in one of the 48 Flash-ADC Fastbus-Modules, which apply zero suppression and fast signal processing in addition to reduce the amount of data to be kept on tape.

Performance as measured during the 161 GeV running in 1996: After modifications in the mechanical support the faces are now stable to better than 5 micron.
Signal-to-noise ratio: $\approx 28:1$ for the $r\phi$ side and $\approx 17:1$ for the z side.
Point resolution achieved: $\sigma_{r\phi} \approx 12\,\mu m$, $\sigma_z \approx 14\,\mu m$ for cos(θ) less than 0.4. These values may improve in the future with more data for the allignment and improvements in the reconstruction algorithms.