DIRAC Experiment
MSGC/GEM Detector
ELECTRONICS

Faustino Gómez Rodríguez
Pablo Vázquez Regueiro

University of Santiago de Compostela, Spain.

December 21, 1999

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For DIRAC experiment [2], 4 MSGC/GEM [3] planes are placed approximately at 2.5 m from the target. Rotated 0, 90, 5 and 85 degrees, each one covers 10.5x10.5 cm^2.

The main purpose of this detector is to provide a direct measurement of the position and the slope of incoming charged tracks before they enter the magnet, independent of the knowledge of the beam position.

1 The MSGC/GEM Electronics

The MSGC/GEM detector readout chain has 3 boards, namely: VME, Control and Mother Board. Their photos are shown in figure 1. The three boards are interconnected through different types of cables, see figure 2.

- Mother-board/Control-board: connected through two (4m length) 40-wires shielded cable.
- Control-board/VME-board: 5 (30m length) twisted-pair coaxial cables. One of them for downloading the control sequence, and the other four for data transmission.

The main characteristics of each board are:

- **Mother Board:** it serves as the mechanical support of the detector. Also the high voltage noise filters, gas pipes and the front-end readout electronics is included in it. This front-end readout electronics is performed by 16 APC SAC 1μm[1], designed by R. Horisberger (from P.S.I. Villigen) and produced by Phillips Faselec.

  The APC (Analog Pipeline Chip) has 64 input channels, each one with a charge sensitive preamplifier followed by an analog pipeline of 32 capacitors. In order to accelerate the readout only 32 channels from each chip [1] are connected to

[1] Actual used channels are #2 to #33. The first channel of each chip is not used.

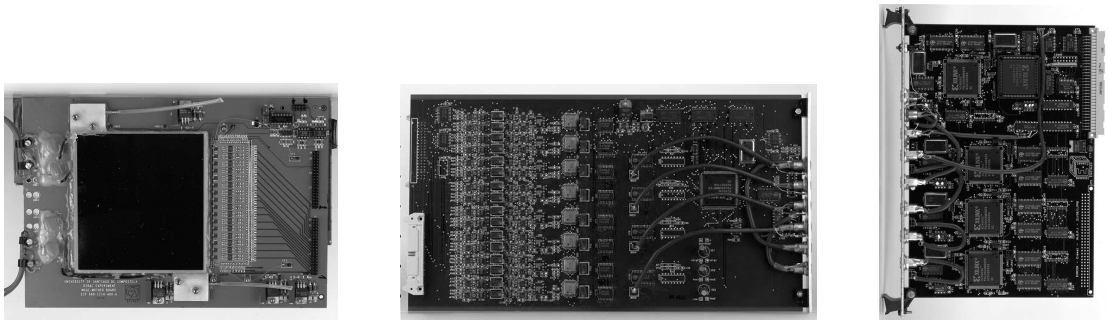

Figure 1: *Photos of the three boards needed for one MSGC readout chain. From the left to the right: Mother, Control and VME Boards.*

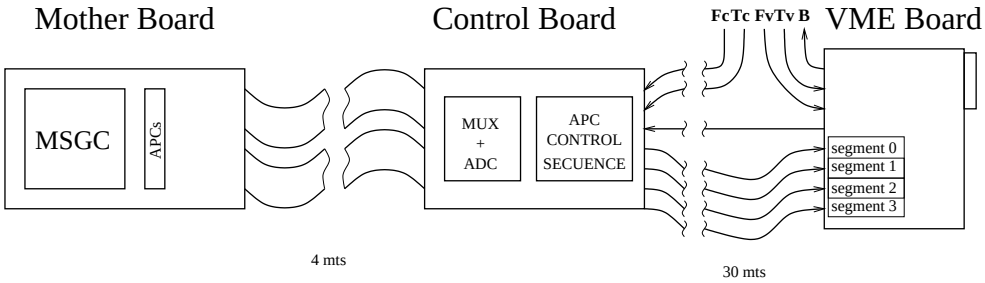

Figure 2: *Scheme of the three boards needed for one MSGC readout chain. Five signals are needed for DAQ:* B: *BUSY,* Tv: *Trigger to VME Board,* Fv: *Fast Clear to VME Board,* Tc: *Trigger to the Control Board,* Fc: *Fast Clear to the Control Board.*

the strips. The APC chips are glued and bonded on a 7-layers ceramic hybrid board. This hybrid is assembled on the Mother Board.

- **Control Board:** the digital sequence needed for the APC control is stored in it. The 512 analog signals from the Mother Board are multiplexed and digitised here. They are sent in groups of 128 to the VME Board.

- **VME Board:** it performs pedestal subtraction and zero suppression. Each VME module is divided in 4 segments that work separately. Each segment is controlled by its own FPGA. When cables between the Control and VME Boards are properly connected, each part of the detector corresponds to a segment as shown in table 2. On any event, every segment receives the digitised pulse height (DPH) of its 128 strips. As soon as a DPH arrives, its corresponding pedestal is subtracted, giving the physical pulse height (PPH) and a counter is incremented, giving the VME strip number. Then the PPH is compared with a threshold. If PPH is equal or greater than threshold, a 2-byte word is written in memory. PPH (1 byte) represents the least significant byte of this word, while the VME strip number corresponds to the most significant byte, see table 7.

  As DPHs arrive multiplexed to the VME Board (figure 4) pedestals must be

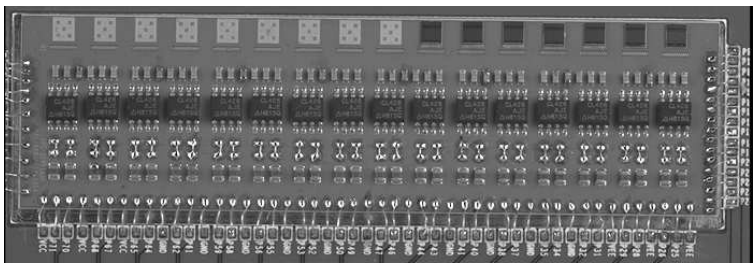

Figure 3: *Ceramic hybrid with the front-end chips.*

stored multiplexed in the same way in Pedestal FIFO memory. The VME strip number is actually the sequential number of the incoming data words. Due to the multiplexing performed in the control board this sequential number no longer corresponds to the detector strip number, see table 1.

1.1 Trigger and Fast Clear

The electronics of the MSGC readout is started by an external trigger signal, and it are able to accept an additional signal, called Fast Clear, that stops the readout of the present trigger, enabling the electronics for new triggers.

Trigger and Fast Clear are handled in parallel by the VME and Control board (this was designed so to avoid time jitters in tele trigger signal arriving to the

segment number	*VME strip*	*Detector strip*	*VME pedestal*	*Detector pedestal*
	0	0	0	0
	1	64	1	64
	2	32	2	32
0	3	96	3	96
	.	.	.	.
	127	127	127	127
	128	128	128	128
	129	128+64	129	128+64
	130	128+32	130	128+32
1	131	128+96	131	128+96
	.	.	.	.
	255	255	255	255
	256	256	256	256
	257	256+64	257	256+64
	258	256+32	258	256+32
2	259	256+96	259	256+96
	.	.	.	.
	383	383	383	383
	384	384	384	384
	385	384+64	385	384+64
	386	384+32	386	384+32
3	387	384+96	387	384+96
	.	.	.	.
	511	511	511	511

Table 1: *Conversion tables: VME strip number to Detector strip number, and VME pedestal number to Detector pedestal number.*

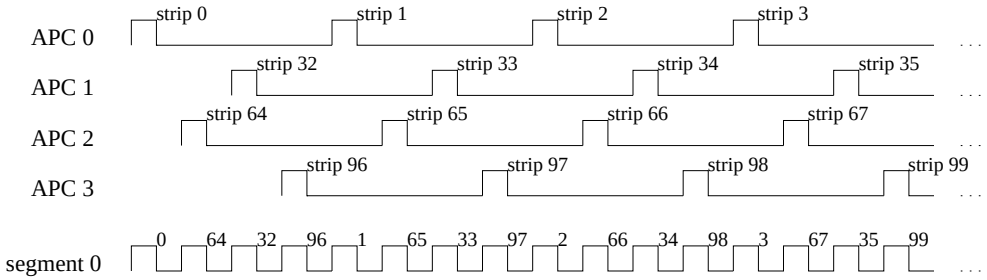

Figure 4: *Strip multiplexing.*

segment	0	1	2	3
channels	0:127	128:255	256:383	384:511

Table 2: *Correspondence between VME Board segment and sector of detector.*

detector). As shown in figure 2 one trigger and one Fast Clear go to the Control Board and the other two copies go to the VME Board. When a trigger arrives to the Control Board, the sampling mode of the APC is stopped, as shown in figure 5. Then, the signal stored in the front-end pipeline is re-read according to an expected trigger delay. After that, sequential readout of the channels in each APC chip is performed, the sixteen APCs are being read at the same time. Finally the APC is reset and a new sampling mode is started. At the end of reset a EOB (End Of Busy) signal is sent from the Control Board to the VME Board.

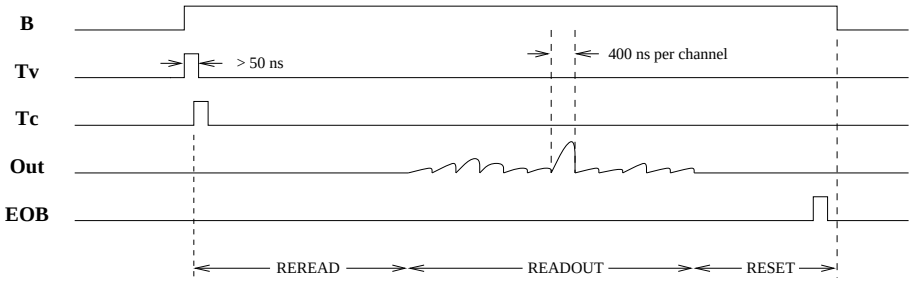

Figure 5: *Timing scheme for MSGC trigger.* B: *Busy,* Tc: *Trigger to the Control Board,* Tv: *Trigger to VME Board,* Out: *One of the four analog output signals,* EOB: *End Of Busy.*

Fast clear must arrive to the Control Board before re-read function is finished, around 12 μs later than trigger arrival. In that case Control Board stops re-read and resets APCs directly.

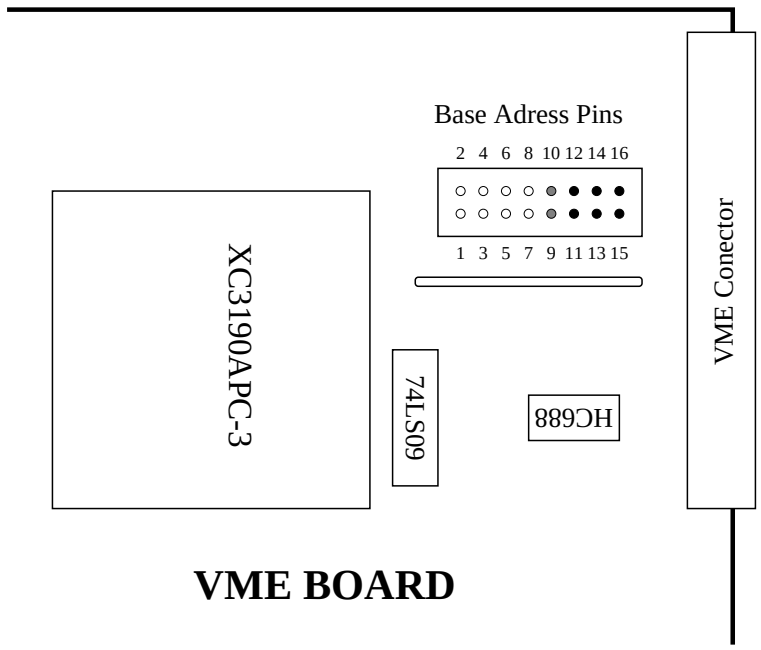

Figure 6: *Base address pins location.*

2 Technical Specifications

Trigger and Fast Clear must be ECL pulses longer than 50 ns. This is due to the internal clock of 20 MHz frequency.

All accesses to the VME Board are implemented in the A24 address space.

2.1 How to Change the VME Module Base Address

Since the DIRAC MSGC sub-detector comprises 4 planes, 4 VME Boards with their 4 base addresses are needed. One VME Board address 256 KBytes (0x40000 bytes), then base addresses must be only selected from 0x000000 to 0xFC0000 in steps of 0x040000. Two examples can be seen in table 3.

plane	*base address*	*pins grounded*	*base address*	*pins grounded*
X	0xF00000	12,11	0xCC0000	13,14
Y	0xF40000	12	0xDC0000	14
U	0xF80000	11	0xEC0000	13
V	0xFC0000	-	0xFC0000	-

Table 3: *Examples of base addresses for the 4 MSGC planes.*

In figure 6 the location on the board of the base address modifier pins can be seen. Pins 1 to 8 are grounded and are meaningless. Pins 9 and 10 are not connected.

The default value of the pins 11 to 16 is 5 Volts, and correspond to address bits as shown in table 4. The default base address for the module is 0xFC0000. To modify this base address, some pins from 11 to 16 must be grounded. Use table 4 for setting different addresses than those shown in table 3.

Pin	16	15	14	13	12	11	-	-	-	...	-
Address bit	A23	A22	A21	A20	A19	A18	A17	A16	A15	...	A0
Default value	1	1	1	1	1	1	0	0	0	...	0
Default value	0xF				0xC				0x0000		

Table 4: *Meaning of the base address pins.*

2.2 Commands

Three access modes are allowed to the VME board into the A24 address space (W8, W16 and R16), see table 5. Commands performed on the board use only these three access modes. We call "command" to a set of one VME memory access, and its address and value associated. A list of valid commands can be seen on the table 6.

W8	8 bits written
W16	16 bits written
R16	16 bits read

Table 5: *Access modes in A24 space.*

2.3 Functions

We call function to a collection of commands that performs a well defined operation on the VME Board. The functions that are needed to operate a MSGC chamber are: *control sequence load, pedestals load, threshold+status register load, board status check, acquisition* and *memory read*, and they are described in paragraphs 2.3.1 to 2.3.6.

2.3.1 Control Sequence Load

APCs control sequence is stored on RAM on the Control board. The control sequence file has 32 rows and a number of lines not fixed. Every line is a command

command			
access	*address*	*value*	*description*
W8	BADD+1	(0:1)	load control sequence on Control Board
W8	BADD	255	stop acquisition, strobe status check
W8	BADD	0	Reset, point memory to BUS VME
W8	BADD	170	point memory to the Control Board
W8	BADD	85	start FIFO pedestals reset
W16	BADD+SO	(0x1FFF)	load threshold+status register
W8	BADD+0x20001	(0:0xFF)	load pedestal
R16	VRA	(0:0xFFFF)	read data memory or status board

Table 6: *Valid commands.* BADD: *base address.* SO: *Segment Offset in {0x0, 0x08000, 0x10000 and 0x18000}.* VRA: *Valid Read Address (all even addresses between BADD and BADD + 0x40000).*

for the Control Board FPGA[2]. Rows are control signals and lines are time steps. Follow command of table 9.

2.3.2 Pedestals Load

It loads the 512 pedestals of a plane in 4 pedestal FIFOs. These pedestal FIFOs[3] are daisy-chained, so only one address has to be written. Pedestals have to be multiplexed in the same order as strips, as shown in table 1, in order to subtract the right pedestal to the right strip in the VME Board. Follow commands of table 10.

2.3.3 Threshold+status Register Load

It loads in a register the threshold and the status for each one of four segments of the VME Board. The meaning of each register bit can be seen in the table 8. Usually this digital threshold and status should be the same in all the segments. The threshold determines whether a channel is stored or not in VME memory. In the status register some parameters of the VME Board are set, namely: The trigger counter can be set so as to increase or not, when a Fast Clear arrives; it can also be set to increase or not when a trigger arrives while the Busy signal is high; the Busy signal is on when a trigger is being processed (fig 5). Optionally the Busy signal can be set to rise or not when the memory is full. Bits 10 and 11 are needed for the board status check. Follow commands of table 11.

[2]Commands in the Control Board are: reset, RAM write, FIFO write, DELAY write, running mode

[3]Each VME segment has its own FPGA and pedestal FIFO.

2.3.4 Acquisition Mode

When control sequence, pedestals and thresholds+status were loaded, memory has to listen to the Control Board. Then MSGC electronics is ready for triggers to be accepted and data to be taken. Follow command of table 12.

2.3.5 Board Status Check

It can be used during the acquisition time, followed by an acquisition mode function, or at the end of an acquisition time, followed by a memory read function. See table 8. Depending on what values were set on bits 10 and 11 of each segment threshold+status register, it can be read: number of words written on that segment, number triggers, content of threshold+status register or value 0. The R16(BASEADD+SO, value) access is used for reading. The W16(BASEADD+SO, thr+st) access is used for changing bits 10 and 11. While this function is used, triggers have to be absent in the VME and Control Boards. Two examples are shown on tables 13 and 14.

In example one, it is assumed that bits 10 and 11 were set to 0 in threshold+status register load. *nwords0, nwords1, nwords2* and *nwords3* are the number of words written in segments 0, 1, 2 and 3 respectively.

In example 2, it is assumed that the bits 10 and 11 were set to 1 and 0 respectively in the threshold+status register load. *thr* is the threshold value in threshold+status register. *A, B* and *E* are the values of bits 8, 9 and 12 in threshold+status register, and they do not change. First W8, stops acquisition. Next six accesses are related to the first memory segment. First R16 gives the threshold+status register value: *thr+AB10E*. Next W16, changes bits 10 and 11 to: *thr+AB01E*, enabling next R16 reads number of triggers: *ntrig0*. Next W16 puts: *thr+AB00E*, enabling next R16 reads number of words written: *nwords0*. Next W16, gives back bits 10 and 11 to their initial values. The same sequence is repeated for segments 1, 2 and 3. It can be checked that all the segments have accepted the same number of triggers.

2.3.6 Memory Read

At the end of a acquisition time, its necessary to know at least how many words have been written in each segment, see 13. After that, each word of each segment can be read with R16 accesses. Follow commands of table 15.

2.4 Data Memory Structure

As it was said before, data memory of MSGC VME Board is physically divided in four segments. Each one has 32 KWords or 64 KBytes and have an offset to base address of: 0, 0x08000, 0x10000 and 0x18000 address positions. Word length is 16 bits. Data memory structure can be seen in table 7

MSB															*LSB*
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	event number														
0	channel number							ADC data							
0	...														
1	event number														
0	channel number							ADC data							

Table 7: *Data memory structure.*

bits	*meaning*								
0:7	threshold								
8	**0**	trigger counter increase with Fast Clear			**1**	no increase			
9	**0**	trigger counter increase with BUSY high			**1**	no increase			
10	**0**	access to	**1**	access to threshold+	**0**	access to	**1**	access to	
11	**0**	memory pointer	**0**	status register	**1**	present trigger	**1**	0 value	
12	**0**	BUSY high after every trigger			**1**	also after memory overflow			

Table 8: *Meaning of threshold+status register bits.*

2.5 External Test Facilities

The MSGC/GEM VME Board has a GREEN LED that lights on bus accesses from or to the board.

2.6 Board Start Up

- Before inserting the board into the crate, make sure the POWER IS SWITCHED OFF.
- Select the base address.
- After a start up of the VME crate, a restart of the Control Board is needed [4].

[4] In this sense, when connecting the readout chain, the Control Board should be switched on **after** the VME crate is switched on and the proper connections between the two boards have been provided.

access	*address*	*value*
W8	BASEADD + 1	data

Table 9: *Command used in* **control sequence load**. data *are digits loaded from file.*

access	*address*	*value*
W8	BASEADD	0
W8	BASEADD	85
W8	BASEADD + 0x20001	ped0
W8	BASEADD + 0x20001	ped2
W8	BASEADD + 0x20001	ped1
W8	BASEADD + 0x20001	ped3
.	.	.
.	.	.
.	.	.
W8	BASEADD + 0x20001	ped511

Table 10: *Commands used in* **pedestal load**. ped *are pedestals multiplexed as shown in table 1.*

access	*address*	*value*
W8	BASEADD	0
W8	BASEADD	255
W16	BASEADD	thr0+st0
W8	BASEADD + 0x10000	255
W16	BASEADD + 0x08000	thr1+st1
W8	BASEADD + 0x20000	255
W16	BASEADD + 0x10000	thr2+st2
W8	BASEADD + 0x30000	255
W16	BASEADD + 0x18000	thr3+st3

Table 11: *Commands used in* **threshold+status register load**. thr0+st0, thr1+st1, thr2+st2 *and* thr3+st3 *are the four possible values for threshold+status register in four segments. Usually these values should be all the same.*

access	*address*	*value*
W8	BASEADD	170

Table 12: *Command to* **start acquisition mode**.

access	*address*	*value*
W8	BASEADD	255
R16	BASEADD	nwords0
R16	BASEADD + 0x08000	nwords1
R16	BASEADD + 0x10000	nwords2
R16	BASEADD + 0x18000	nwords3

Table 13: *Commands used in a* **board status check**, *example one.*

access	*address*	*value*
W8	BASEADD	255
R16	BASEADD	thr+AB10E
W16	BASEADD	thr+AB01E
R16	BASEADD	ntrig0
W16	BASEADD	thr+AB00E
R16	BASEADD	nwords0
W16	BASEADD	thr+AB10E
R16	BASEADD + 0x08000	thr+AB10E
W16	BASEADD + 0x08000	thr+AB01E
R16	BASEADD + 0x08000	ntrig1
W16	BASEADD + 0x08000	thr+AB00E
R16	BASEADD + 0x08000	nwords1
W16	BASEADD + 0x08000	thr+AB10E
R16	BASEADD + 0x10000	thr+AB10E
W16	BASEADD + 0x10000	thr+AB01E
R16	BASEADD + 0x10000	ntrig2
W16	BASEADD + 0x10000	thr+AB00E
R16	BASEADD + 0x10000	nwords2
W16	BASEADD + 0x10000	thr+AB10E
R16	BASEADD + 0x18000	thr+AB10E
W16	BASEADD + 0x18000	thr+AB01E
R16	BASEADD + 0x18000	ntrig3
W16	BASEADD + 0x18000	thr+AB00E
R16	BASEADD + 0x18000	nwords3
W16	BASEADD + 0x18000	thr+AB10E

Table 14: *Commands used in a* **board status check**, *example two.*

access	*address*	*value*
W8	BASEADD	0
R16	BASEADD	data
.	.	.
R16	BASEADD + nwords0	data
R16	BASEADD + 0x08000	data
.	...	.
R16	BASEADD + 0x08000 + nwords1	data
R16	BASEADD + 0x10000	data
.	...	.
R16	BASEADD + 0x10000 + nwords2	data
R16	BASEADD + 0x18000	data
.	...	.
R16	BASEADD + 0x18000 + nwords3	data

Table 15: *Commands used in* **memory read**. *W8(255) stops acquisition and enables readout.* data *have structure of table 7.*

References

[1] **A novel readout chip for silicon strip detectors with analog pipeline and digitally controlled analog signal processing**. R. Horisberger (Paul Scherrer Institute). D. Pitzl (Institute fur Mittelenerhiephysik, EHT Zurich). NIM A326 (1993) 92-99

[2] **Proposal to the SPSLC: Lifetime Measurements of $\pi^+\pi^-$ Atoms to Test Low Energy QCD Predictions**. CERN/SPSLC 95/1, SPSLC/P284 updated 10 Nov 1995

[3] **Performance of MSGC with Analog pipeline Readout**. F. Gómez, B. Adeva, G. Gracia, M.A. López, T. Núñez, A. Pazos, M. Pló, A. Rodríguez, C. Santamarina, P. Vázquez (Santiago de Compostela U.). 1997. Published in NIM A384 (1997) 351-359