European Organization for Nuclear Research
Organisation européenne pour la recherche nucléaire

CERN Doctoral student project proposal:

Radiation-hardened Field Programmable Gate Arrays in deep submicron CMOS process

This Ph.D. project aims to research and develop a radiation-hardened Field Programmable Gate Array (FPGA) to be used in detector systems for future experiments at the Large Hadron Collider at CERN. The scope of the project includes the study of FPGA architectures, the study of radiation effects (SEU/SET/TID), microelectronic circuit design and implementation, functional evaluation, and radiation qualification of the prototyped circuits. The project will also require development or adaptation of dedicated Computer-Aided Design (CAD) software capable of synthesizing, mapping, and place and routing user designs to the proposed FPGA architecture.

The Ph.D. candidate will be given the opportunity to steer and refine the research based on their specific background and interests in consultation with their supervisor. Contributions to established open source software projects in this area (see examples below) as well as their use in the project will be encouraged.

We are looking for a candidate with a solid background in Electronic Engineering or Computer Science. An experience in microelectronics and programming (e.g. C/C++, python) is considered a plus.

If you are interested in the project and would like to have more information please contact Dr Szymon Kulis (szymon.kulis@cern.ch). General information about the Doctoral Student Programme at CERN can be found at https://careers.cern/students.

References:
- Verilog-to-Routing (https://github.com/verilog-to-routing/vtr-verilog-to-routing)
- yosys (https://github.com/YosysHQ/yosys)
- nextpnr (https://github.com/YosysHQ/nextpnr)
- OpenFPGA (https://github.com/LNIS-Projects/OpenFPGA)