

Table of Contents

1. INTRODUCTION	1
1.1. SCOPE OF THE TDR	1
1.2. FORMAT OF THE TDR	1
2. REQUIREMENTS (BEAT/CLARA)	2
2.1. PHYSICS REQUIREMENTS	2
2.2. REQUIREMENT FROM EXTERNAL SUB-SYSTEMS	2
2.2.1. <i>LHCb Detector</i>	3
2.2.2. <i>LHCb Trigger System</i>	3
2.2.3. <i>Running Modes and Partitioning</i>	3
2.2.4. <i>Data Processing and Offline Computing</i>	4
2.2.5. <i>LHC Accelerator</i>	4
2.2.6. <i>Infrastructure Services</i>	5
2.2.7. <i>Detector Safety</i>	5
2.2.8. <i>Experiment Operations</i>	5
2.3. SYSTEM REQUIREMENTS	5
2.3.1. <i>Functional Requirements</i>	5
2.3.2. <i>Performance Requirements</i>	6
3. SYSTEM DESIGN	7
3.1. DESIGN PRINCIPLES AND CONSTRAINTS	7
3.2. ARCHITECTURE AND PROTOCOLS (BEAT)	7
3.3. TIMING AND FAST CONTROLS (RICHARD J.)	8
3.4. DATAFLOW SYSTEM (BEAT)	8
3.4.1. <i>Front-End Multiplexer Layer</i>	8
3.4.2. <i>Readout Unit Layer</i>	9
3.4.3. <i>Readout Network Layer</i>	9
3.4.4. <i>Sub-Farm Controller Layer</i>	9
3.4.5. <i>Data-Flow Protocol and Traffic Control</i>	9
3.5. EVENT FILTER FARM (BEAT, NIKO, PHILIPPE G.)	10
3.6. EXPERIMENT CONTROL SYSTEM (CLARA)	10
3.7. DISCUSSION	10
3.7.1. <i>Dataflow System</i>	10
3.7.2. <i>Experiment Control System</i>	10
4. SYSTEM IMPLEMENTATION AND REALISATION	11
4.1. TIMING AND FAST CONTROLS	11
4.2. DATAFLOW	11
4.2.1. <i>Data Link Technology</i>	11
4.2.2. <i>Front-End Multiplexing and Readout Units</i>	11
4.2.3. <i>Event Building</i>	13
4.3. EVENT FILTER FARM	13
4.4. CONTROLS INTERFACE TO ELECTRONICS	13
4.4.1. <i>SPECS</i>	13
4.4.2. <i>ELMB</i>	13
4.4.3. <i>Credit-Card PCs</i>	14
4.5. EXPERIMENT CONTROL SYSTEM	14
4.5.1. <i>System Configuration (Beat/Clara)</i>	14
4.5.2. <i>Detector Conditions and Status (Beat/Clara)</i>	14
4.5.3. <i>Data Quality Monitoring (Beat)</i>	14
4.5.4. <i>Bookkeeping and Connection to Offline Computing (Beat)</i>	14
4.5.5. <i>Controls Software Framework and Tools (Clara)</i>	14
4.6. SCALE OF THE SYSTEM (NIKO, CLARA, BEAT, ETC...)	14
4.7. ONLINE COMPUTING INFRASTRUCTURE	15

4.7.1.	<i>Computing and Network Infrastructure (Beat/Philippe G.)</i>	15
4.7.2.	<i>Power and Cooling (Philippe G.)</i>	15
4.7.3.	<i>Location of Equipment (Beat/Clara/Philippe G.)</i>	15
4.7.4.	<i>Control Room (Beat/Clara/Philippe G.)</i>	15
4.7.5.	<i>Connection to Cern Computer Centre (Beat/Philippe G.)</i>	15
5.	INTEGRATION AND COMMISSIONING	16
6.	COST, PLANNING AND RESPONSIBILITIES	17
6.1.	DATA ACQUISITION COST (BEAT/NIKO).....	17
6.2.	EXPERIMENT CONTROL SYSTEM COST (BEAT/CLARA).....	17
6.3.	PLANNING (BEAT/CLARA)	17
6.3.1.	<i>Implementation</i>	17
6.3.2.	<i>Integration and Commissioning</i>	17
6.4.	RESPONSIBILITIES (BEAT/CLARA)	17
APPENDIX A.	FRONT-END MULTIPLEXING R&D STUDIES	18
A.1.	FPGA-BASED FEM/RU (HANS M.)	18
A.2.	NETWORK PROCESSOR-BASED FEM/RU (NIKO).....	18
A.2.1	<i>Ingress Event Building</i>	19
6.4.1.	<i>Egress Event Building</i>	19
6.4.2.	<i>Benchmarking</i>	20
A.2.4	<i>Measurements with the Reference Platform</i>	20
APPENDIX B.	EVENT-BUILDING R&D STUDIES	22
B.1.	MYRINET STUDIES (BEAT).....	22
B.2.	GIGABIT ETHERNET STUDIES.....	22
B.3.	“SMART” NIC STUDIES.....	24
B.4.	NETWORK TOPOLOGY STUDIES (JEAN-PIERRE)	25
APPENDIX C.	TEST-BEAM ACTIVITIES (CLARA/SASCHA/RICHARD B.)	27