AX-PET DAQ/Analysis meeting
06/5/09 – 512-R-004

Present: V.Fanti, E.Chesi, P.Weilhammer, A.Rudge, P.Solevi, C.Joram, P.Beltrame.

Agenda:
- Light yields in WLS as a function of WLS multiplicity: results from analysis of run with higher MPPC voltage.

Measurements with 300 mV additional voltage to MPPC

Measurements description:
- Measurements performed with the new trigger system in Bdg 28
- I layer in standard conditions
- II layer with black separators between crystals

Results:
- Dependence of LYSO and WLS multiplicity on the delay: plateau for LYSO and WLS at dt < 40 ns and dt < 20 ns respectively.
- Multiplicity in WLS goes up with increasing voltage by 300 mV.
- WLS multiplicity goes from 2.4 to 1.5 (dt < 20 ns) in the I and II layer respectively.
- No saturation in ADC counts observed in the WLS spectra even at + 300 mV.
- The increase of the mean ADC counts vs WLS multiplicity still present:

	I layer (no black)	II layer (with black)
WLS # 1	319	225
WLS # 2	479	350
WLS # 3	639	458

Outcomes of the discussion:
- From 20 ns down with +300 mV stability is achieved with respect to both LYSO and WLS.
- Similar behavior can be expected by operating the MPPCs at nominal bias but lowering the threshold.
- The black separators reduce both multiplicity and average light collected of WLS strips, but 50% increase of signal remains (only 25% increase observed in simulations with 4 cm long WLS and 1 LYSO).
- Possible explanation: pedestal not properly subtracted. It has to be confirmed by performing an acquisition in serial mode without pedestal subtraction -> take off the signal -> analyze pedestals (if Gaussian etc.).

Planned measurements

1) Serial mode, no discriminator, minimum delay (dt = 4 ns), nominal bias, no pedestal subtraction,100 K events.
2) Serial mode, with discriminator, minimum delay, nominal bias, no pedestal subtraction, 100 K events.
3) Serial mode, no discriminator, minimum delay, nominal bias, no pedestal subtraction, no data lock, 100 K events.
4) Sparse mode, minimum delay, nominal bias, pedestal subtraction, lower threshold (40 mV, 60 mV and 80 mV).

Acquisitions will be performed by using Viviana DAQ code.

Few remarks on Bdg 304

- Thomas has started assembling layer II on Monday. He hopes to finish full module next week.
- It has to be checked if cables are long enough to put power supply outside.