Dual RF power detector optimized for pulsed signals

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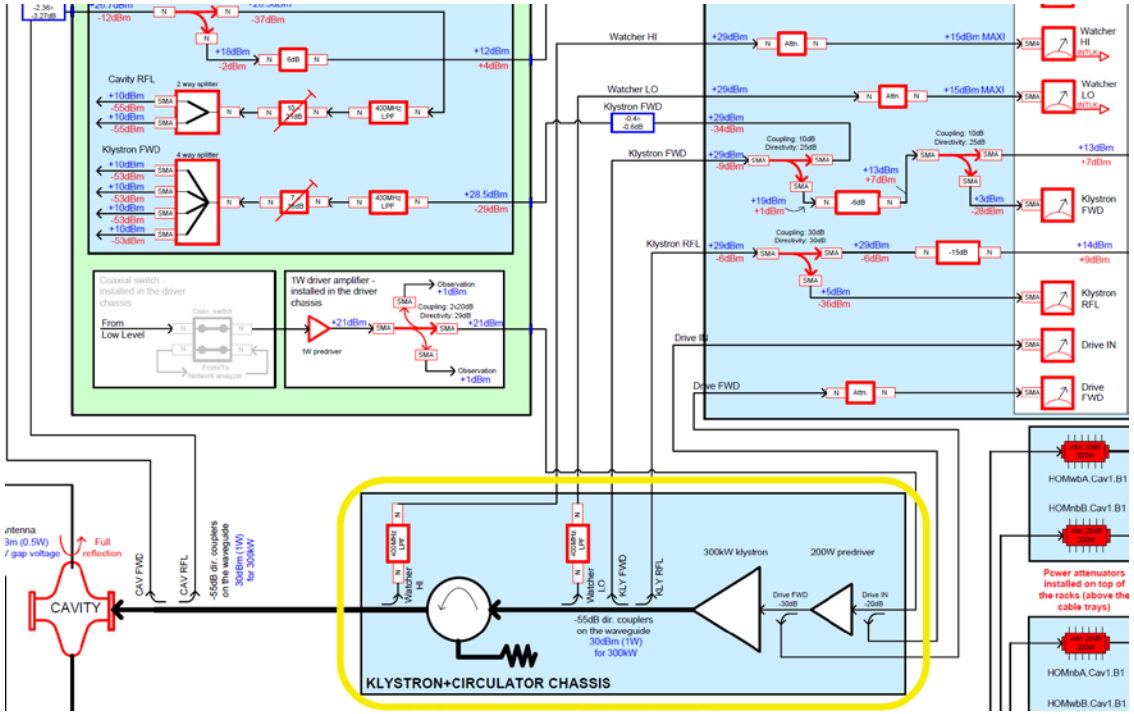
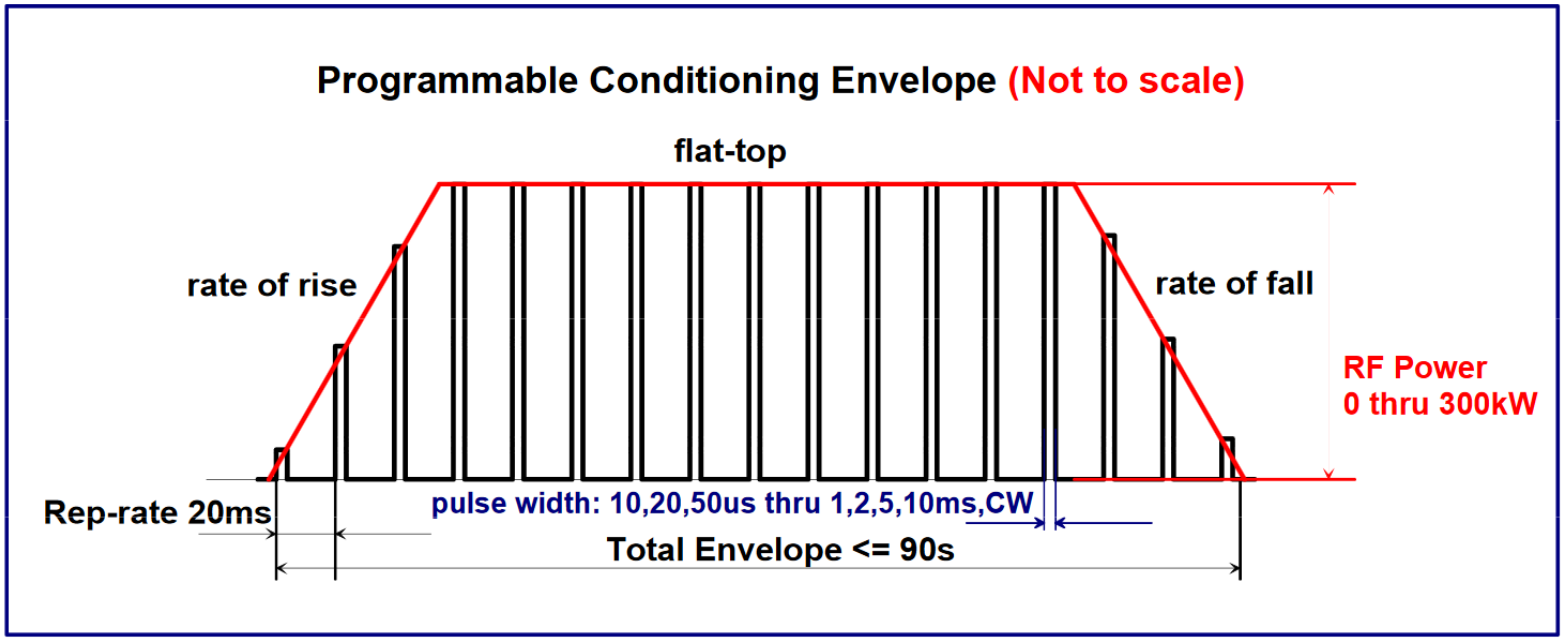
Motivation

- Measurement of RF power during the cavity conditioning in the LHC
- By measuring the forward and reflected power we can control the circulator bias current and minimize power reflected back to the klystron



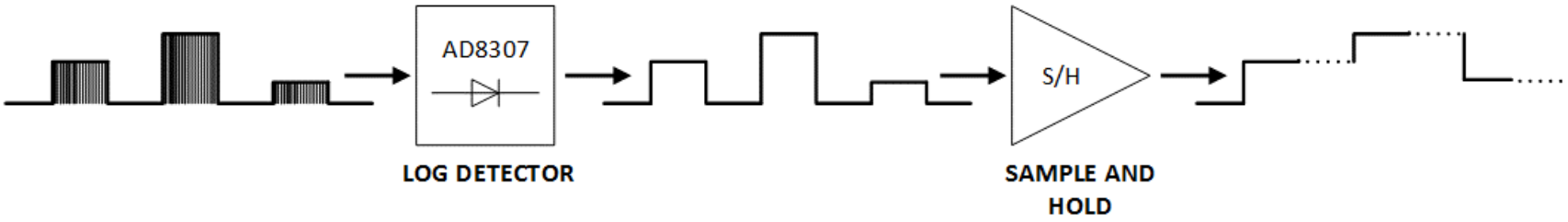
Motivation

- The current version of the Power meter works fine in continual wave operation
- For optimal tuning of the circulator during the cavity conditioning we have to measure the power also in pulsed mode

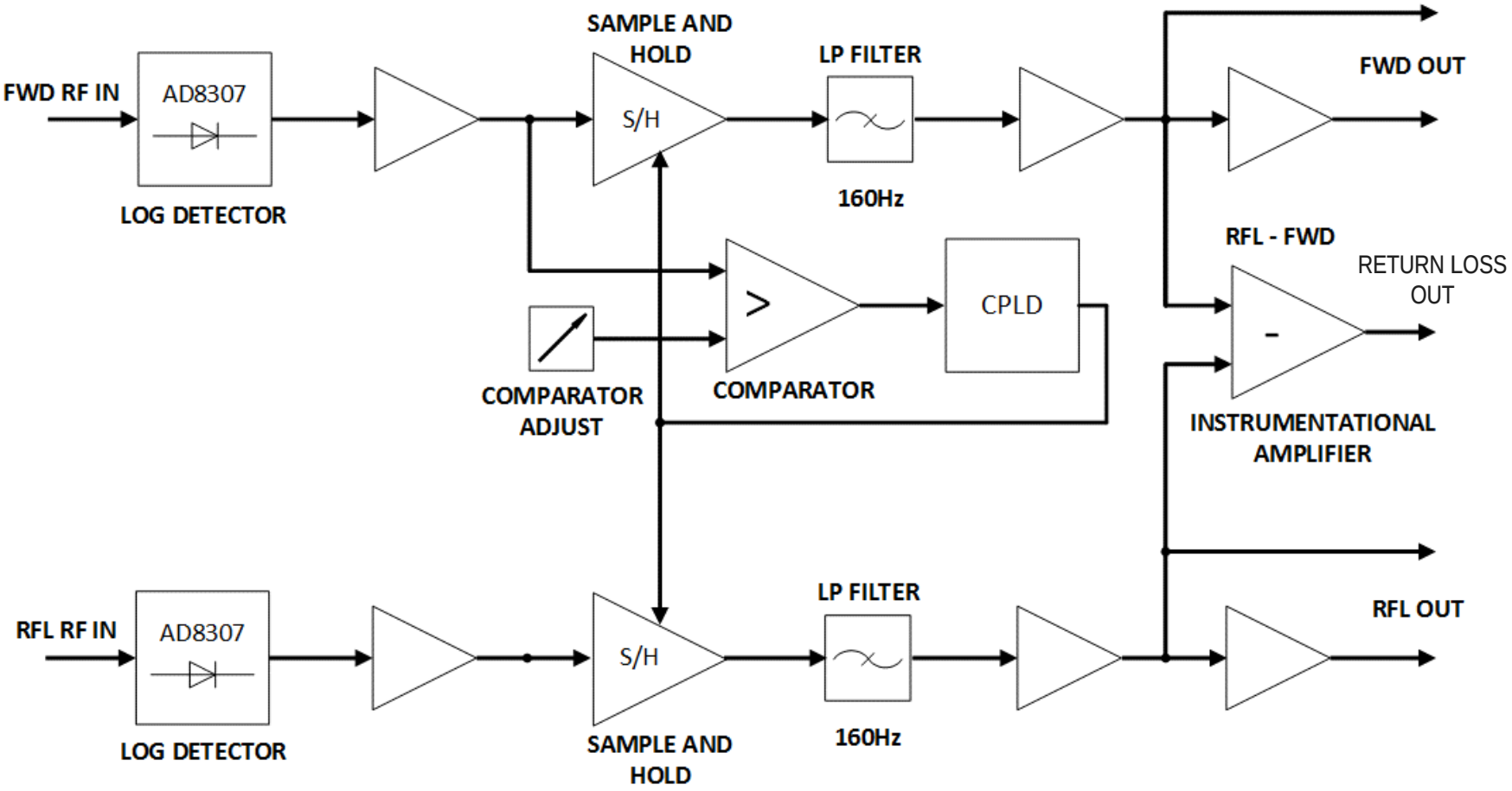


Requirements

- Fully compatible with the current “Dual RF power meter” (AED-00045)
- Abbility to measure the power of pulses with lenght from 50 µs with repetition rate of 50 Hz to continual wave
- Maximum input power +15 dBm
- >60 dB dynamic range
- 0-10 V outputs to the PLC

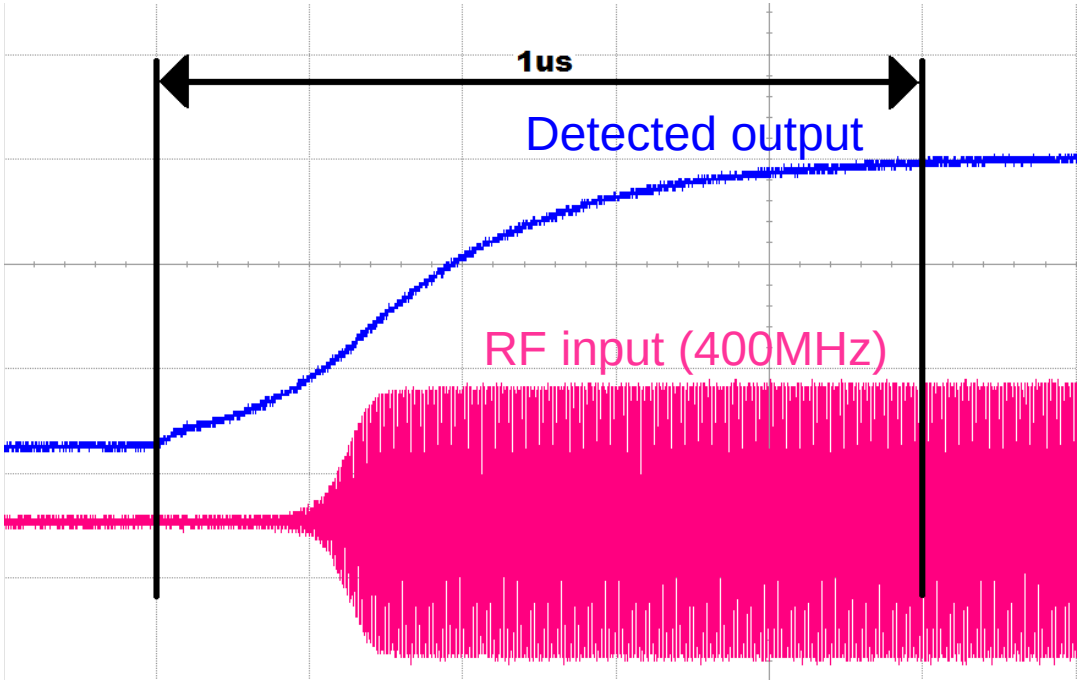


Block diagram



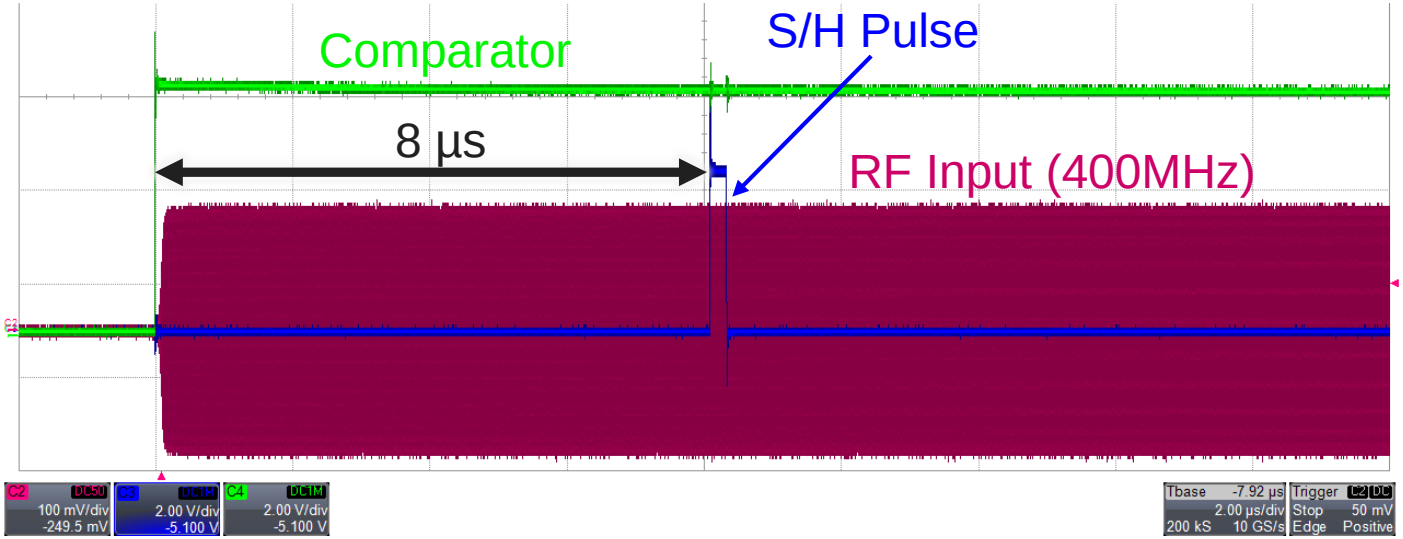
RF Power detection

- AD8307 logarithmic detectors used
- 90 dB dynamic range
- Good response for rising edge ~1 µs
- ~20 mV per dBm output



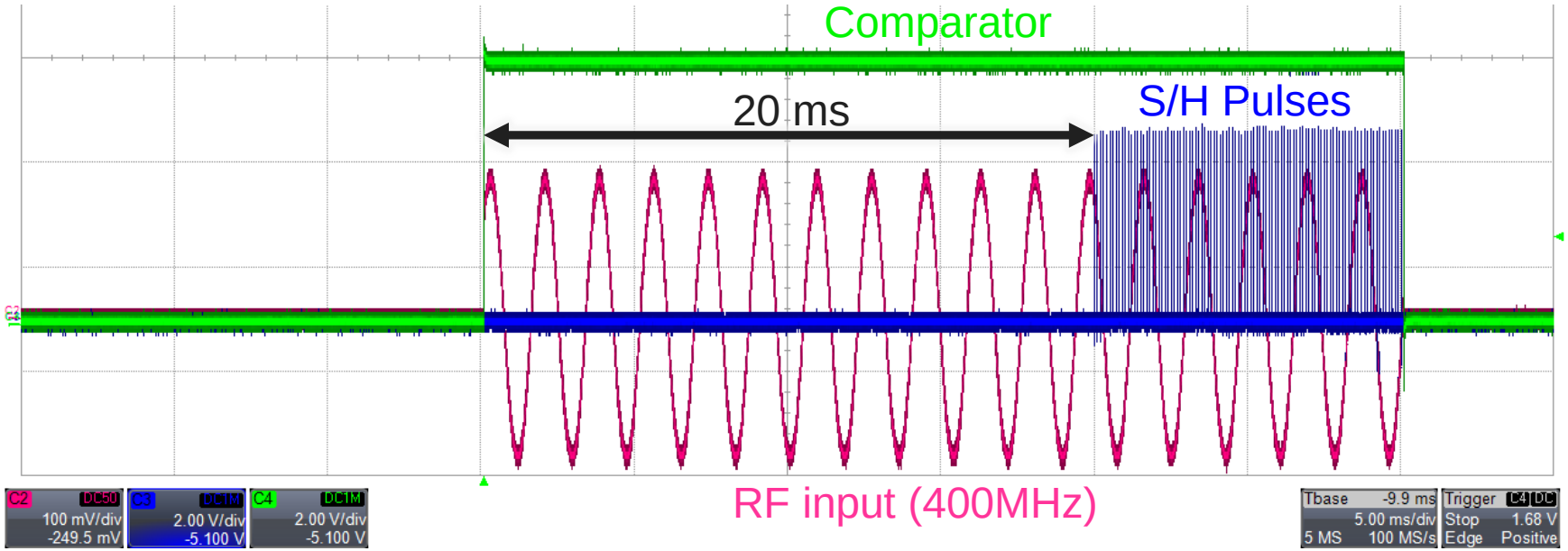
Detector operation in pulsed mode

- Peak detector can’t be used because we need to capture the amplitude
- The PLC sampling frequency is low therefore we must hold the detector readings between the pulses
- Pulse amplitude should be stable after a few µs, so we choose 8 µs delay for the S/H pulse



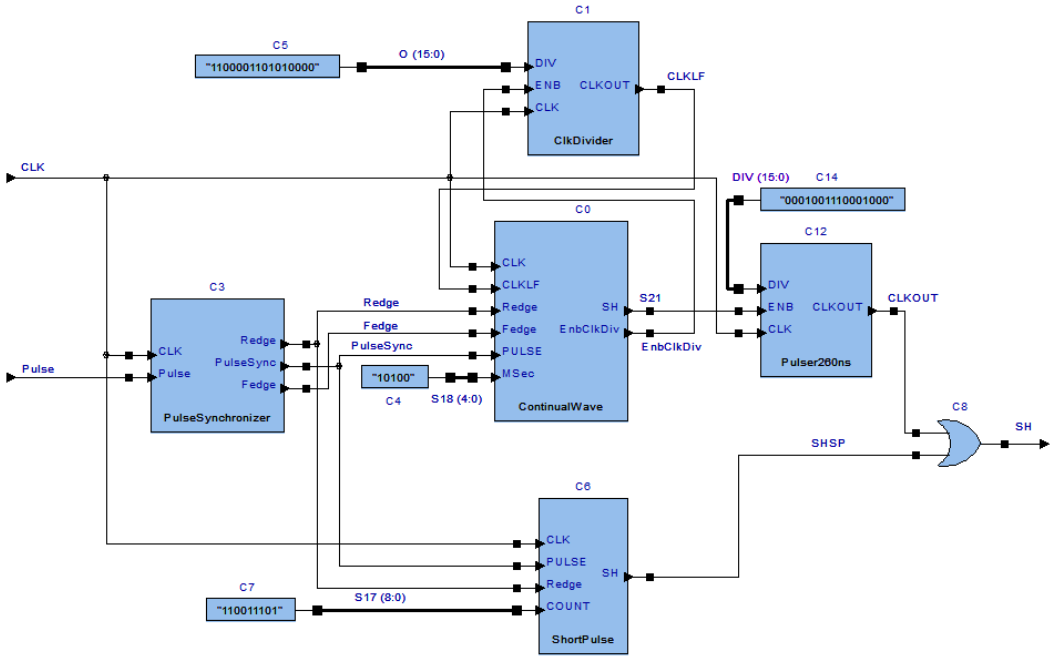
Continual wave operation

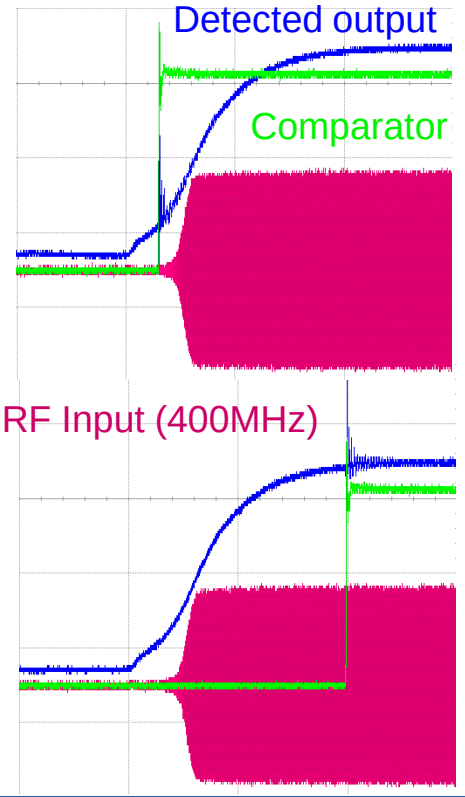
- The repetition rate of pulses during the cavity conditioning is 50 Hz, therefore if wave lasts longer than 20 ms its considered as CW
- S/H amp can't accurately represent the input, so we apply S/H pulses every 100 µs



CPLD and Pulse detection

- Comparator used as a pulse detector
- Comparator threshold level can be adjusted by trimmer
- S/H signal driving are provided by Xilinx XC2C256 CPLD

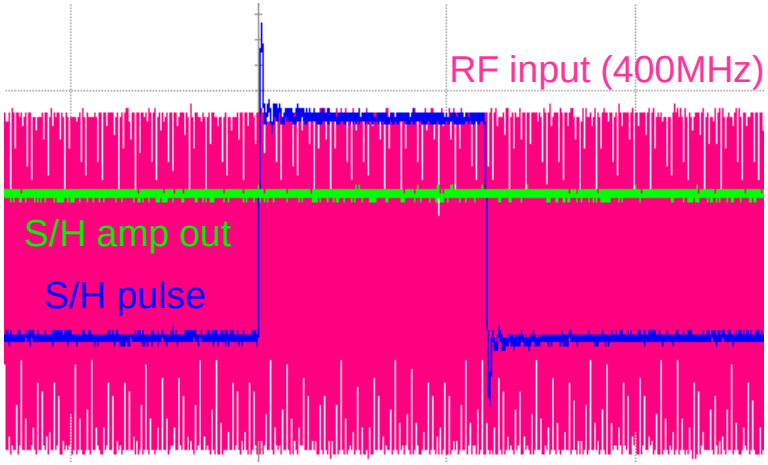


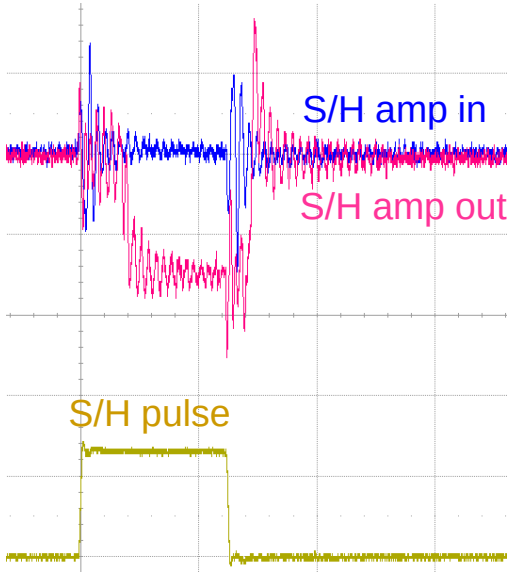


LP filter and Analogue return loss calculation

- Low pass filter with cutoff frequency of 160 Hz filters noise from the signal sampling
- Instrumentational amplifier subtracts FWD and RFL signals to provide the analogue return loss output

$$RL(dB) \cong \log(RFL) - \log(FWD)$$

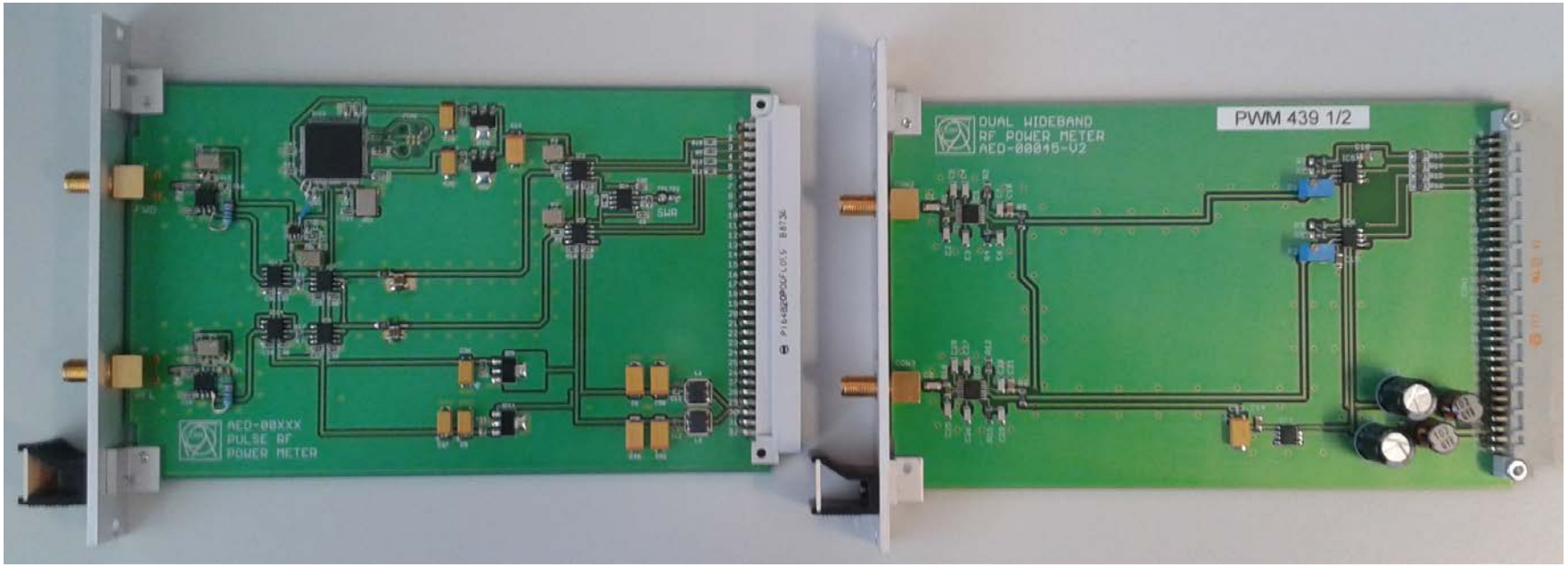




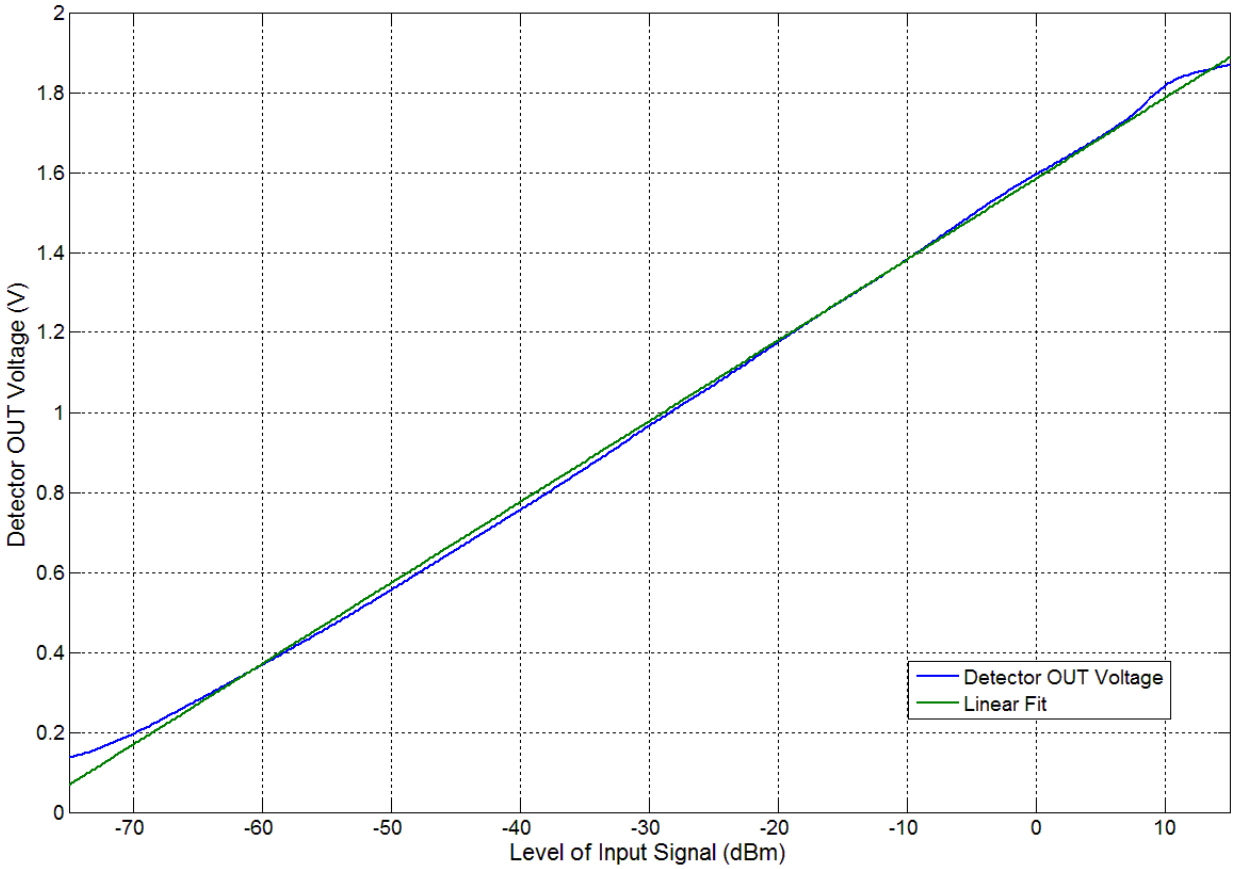
Boards comparision

New version of Power detector

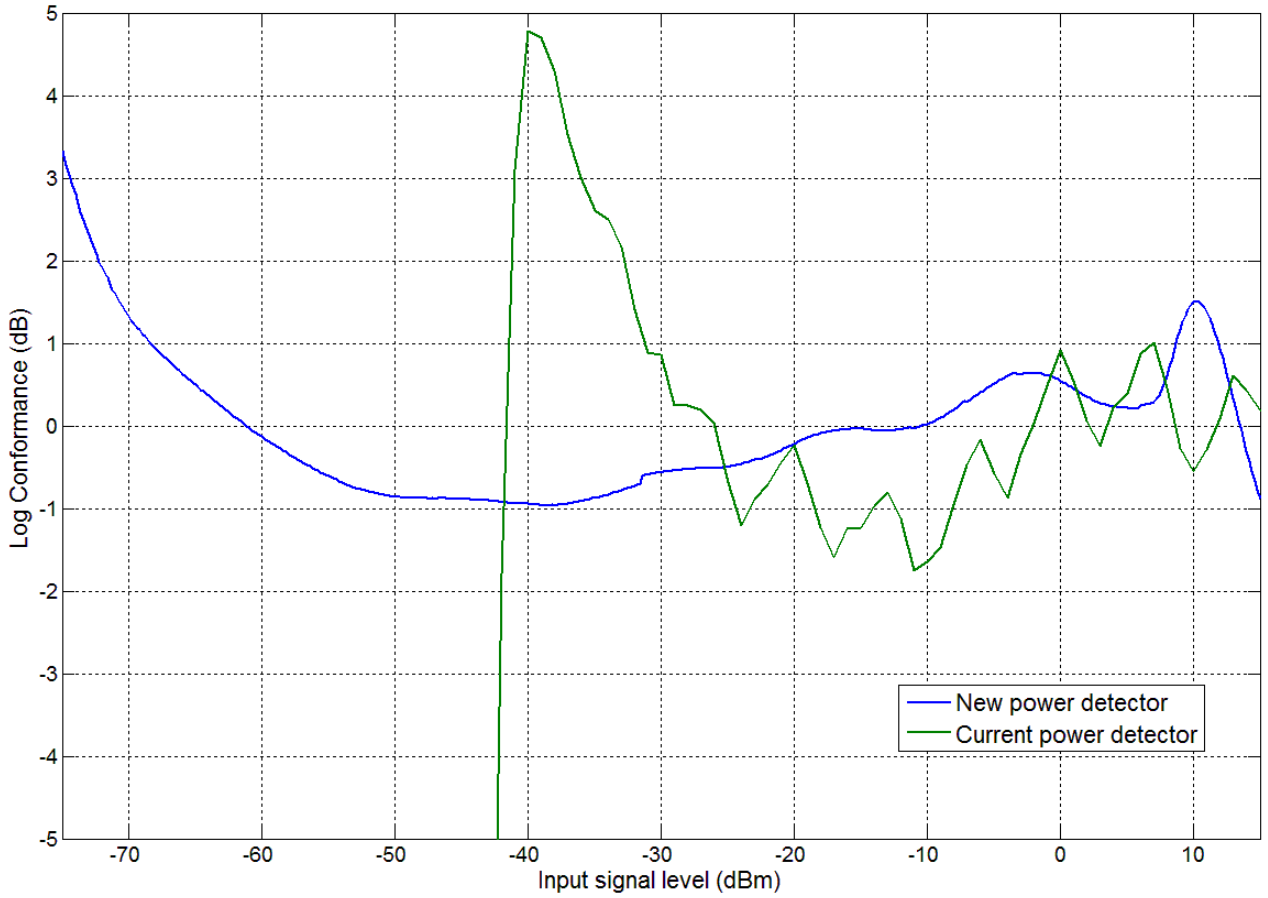
Currently used Dual wideband RF power meter (AED-00045)



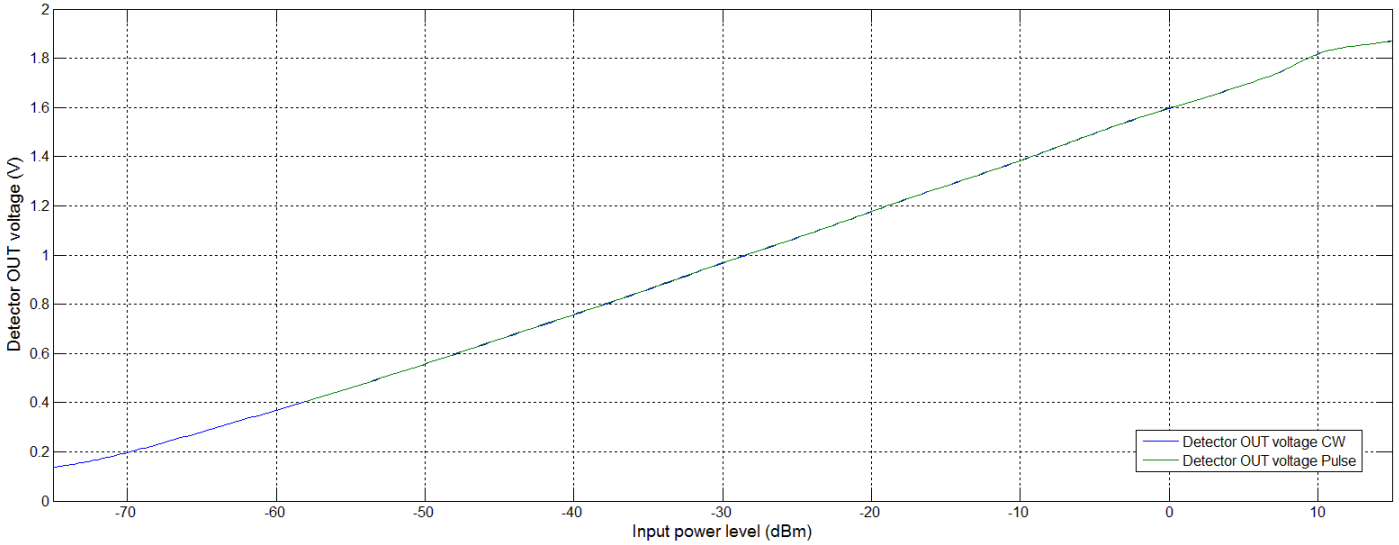
Transfer chracteristic

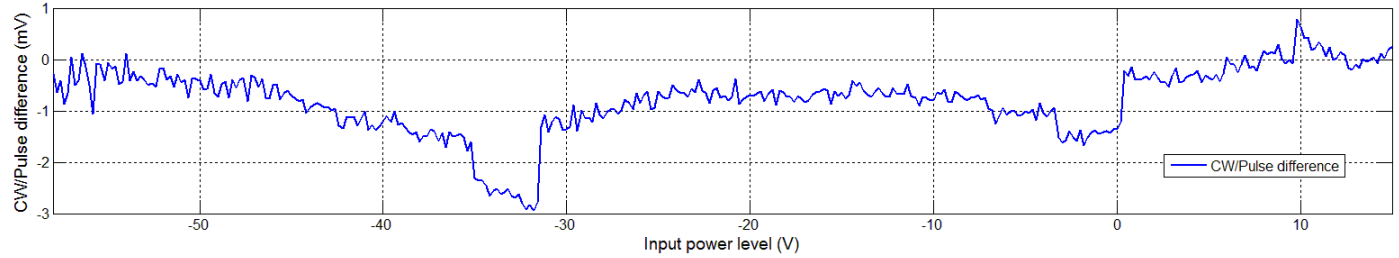


Log conformance comparision



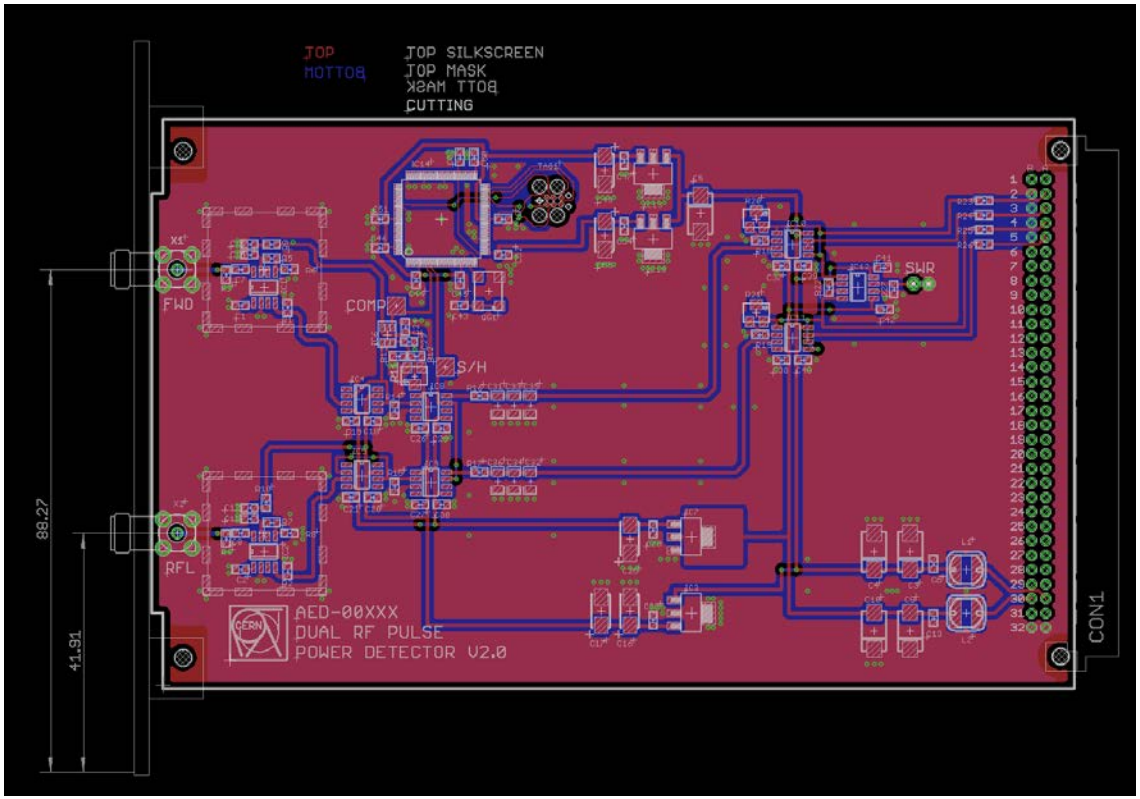
CW and Pulse mode comparision



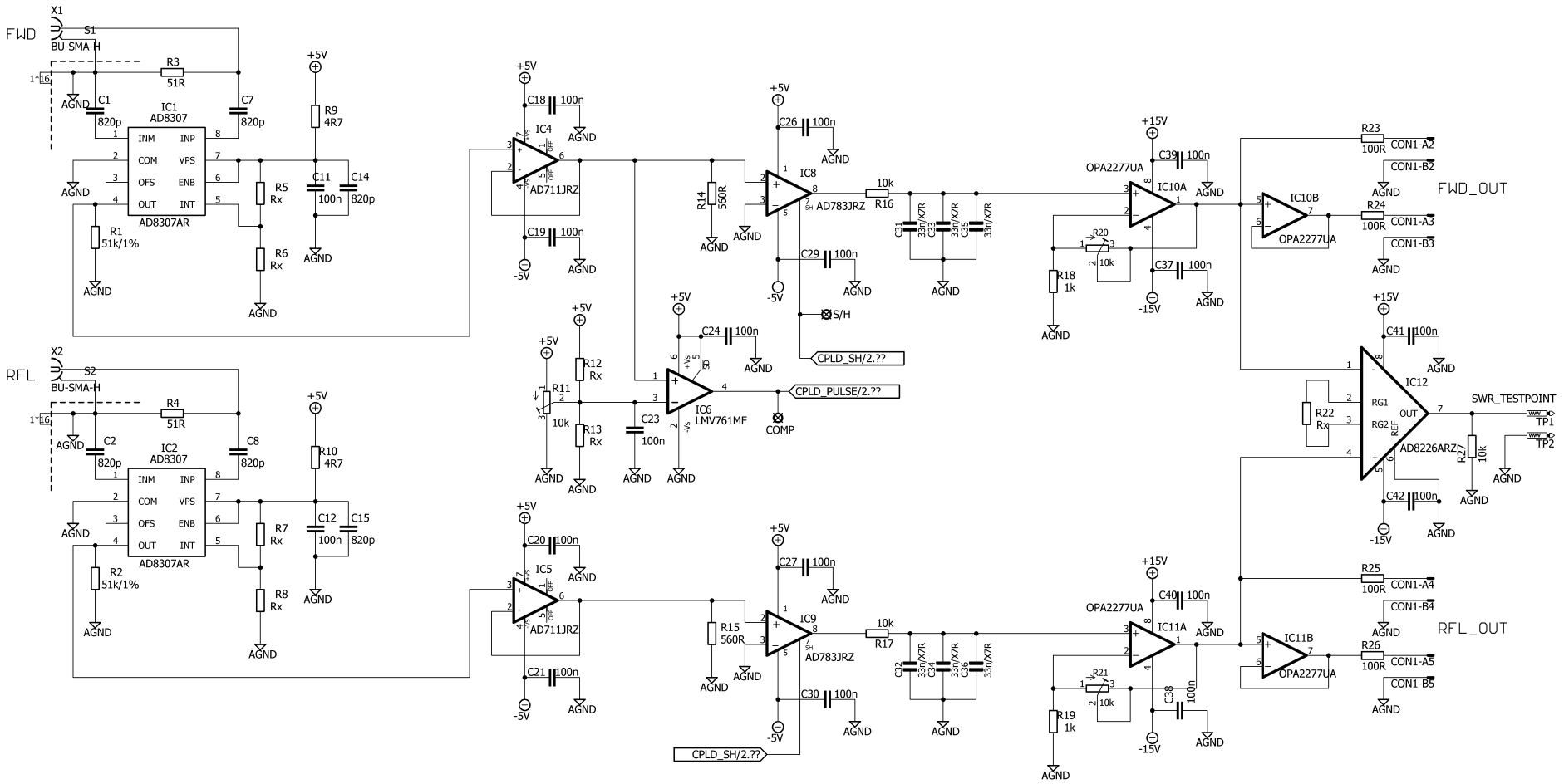


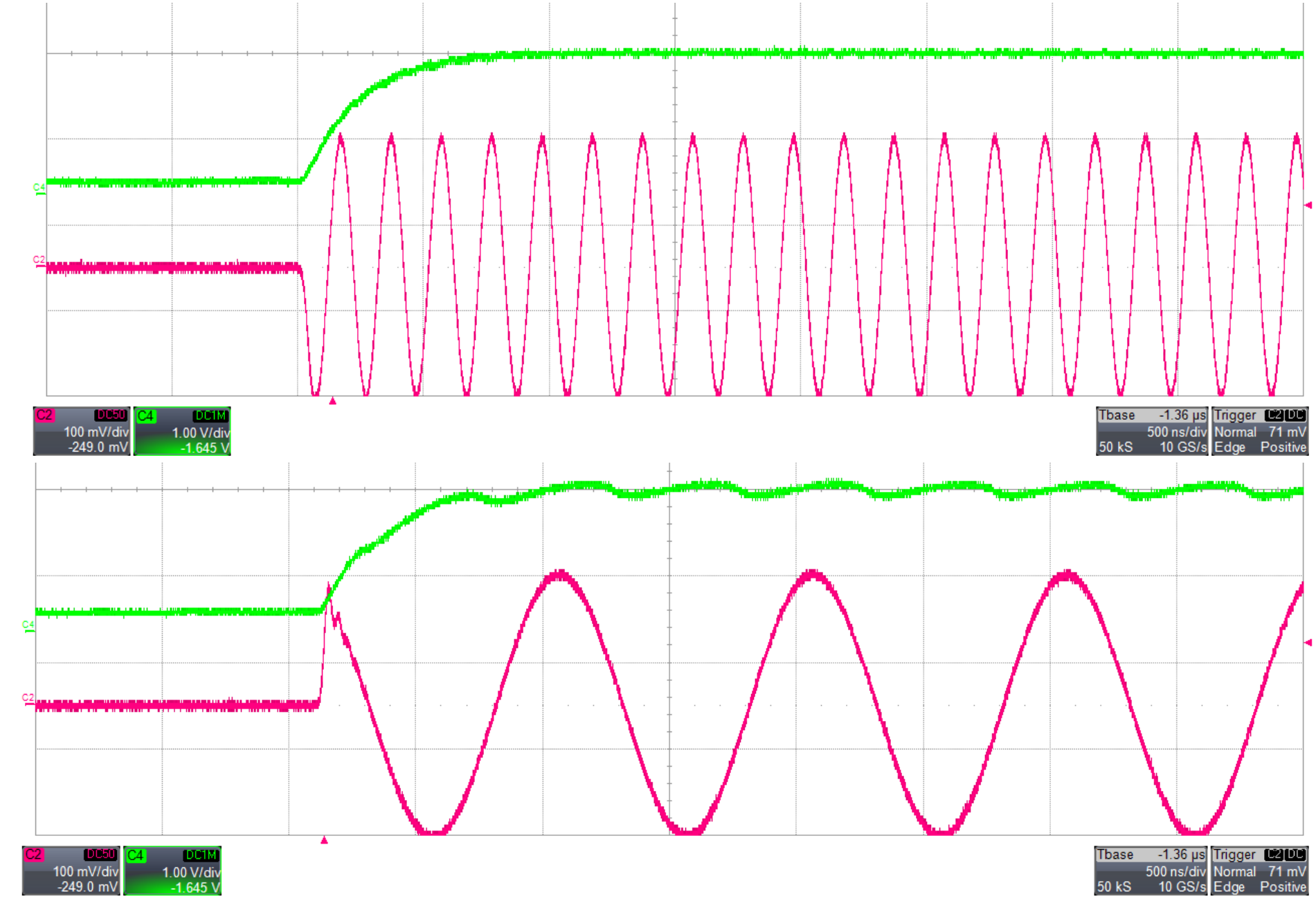
Project status

- Version 2 of the board designed and ready to be sent for production
- Prototype successfully tested
- Characteristics measured



Thank you for your attention


FWD
RFL
X1
X2
S1
S2
BU-SMA-H
R3
R4
51R
IC1
IC2
AD8307
AD8307AR
INM
INP
COM
VPS
OFS
ENB
OUT
INT
C1
C2
C7
C8
820p
R1
R2
51k/1%
R5
R6
R7
R8
Rx
C11
C12
C14
C15
100n
R9
R10
4R7
+5V
-5V
AGND
IC4
IC5
AD711JRZ
C18
C19
C20
C21
100n
R14
R15
560R
IC8
IC9
AD783JRZ
C26
C27
C29
C30
S/H
R16
R17
10k
C31
C32
C33
C34
C35
C36
33n/X7R
OPA2277UA
IC10A
IC10B
IC11A
IC11B
C39
C40
C37
C38
R18
R19
1k
R20
R21
-15V
+15V
FWD_OUT
RFL_OUT
R23
R24
R25
R26
100R
CON1-A2
CON1-B2
CON1-A3
CON1-B3
CON1-A4
CON1-B4
CON1-A5
CON1-B5
IC6
LMV761MF
C24
R11
R12
R13
C23
CPLD_SH/2.??
CPLD_PULSE/2.??
COMP
IC12
AD8226ARZ
RG1
RG2
REF
OUT
R22
R27
SWR_TESTPOINT
TP1
TP2
C41
C42


C4
C2
C2 DC50
100 mV/div
-249.0 mV
C4 DC1M
1.00 V/div
-1.645 V
Tbase -1.36 µs
500 ns/div
50 kS 10 GS/s
Trigger C2 DC
Normal 71 mV
Edge Positive
C4
C2
C2 DC50
100 mV/div
-249.0 mV
C4 DC1M
1.00 V/div
-1.645 V
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