Thermal compensation of SPS optical delay lines

Reference signal distribution within the LLRF lab complex

SPS damper pickup and test point signal fan-out

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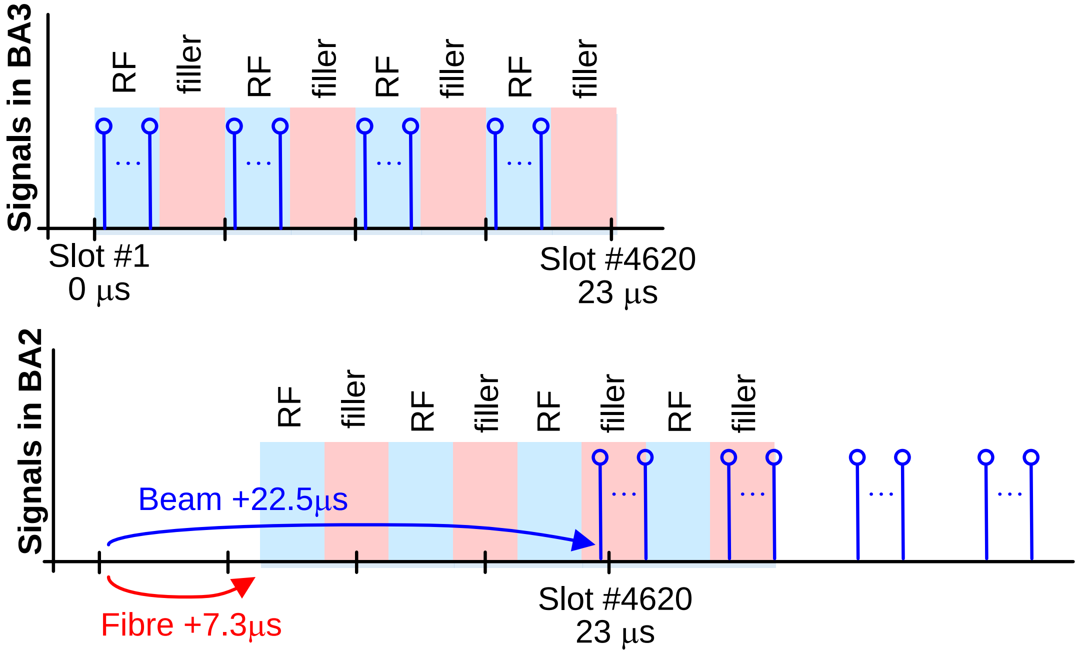
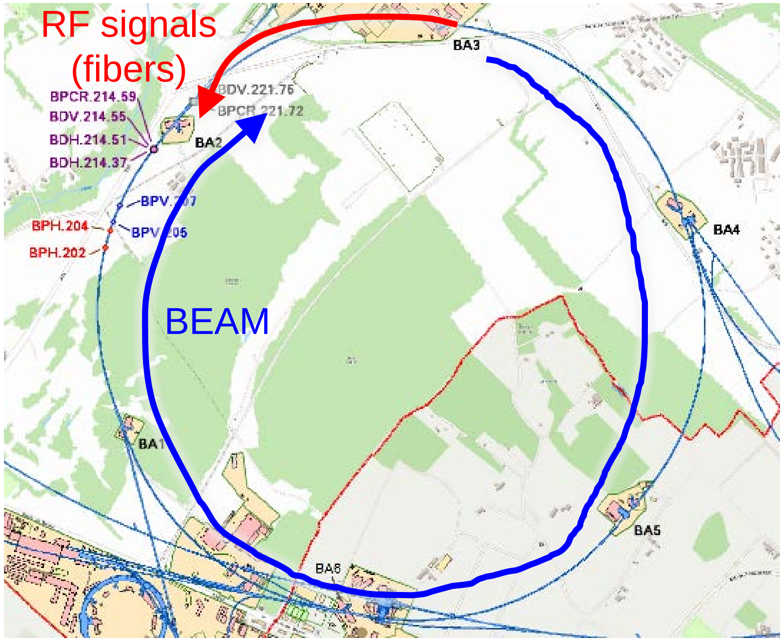
25. August 2016

Motivation

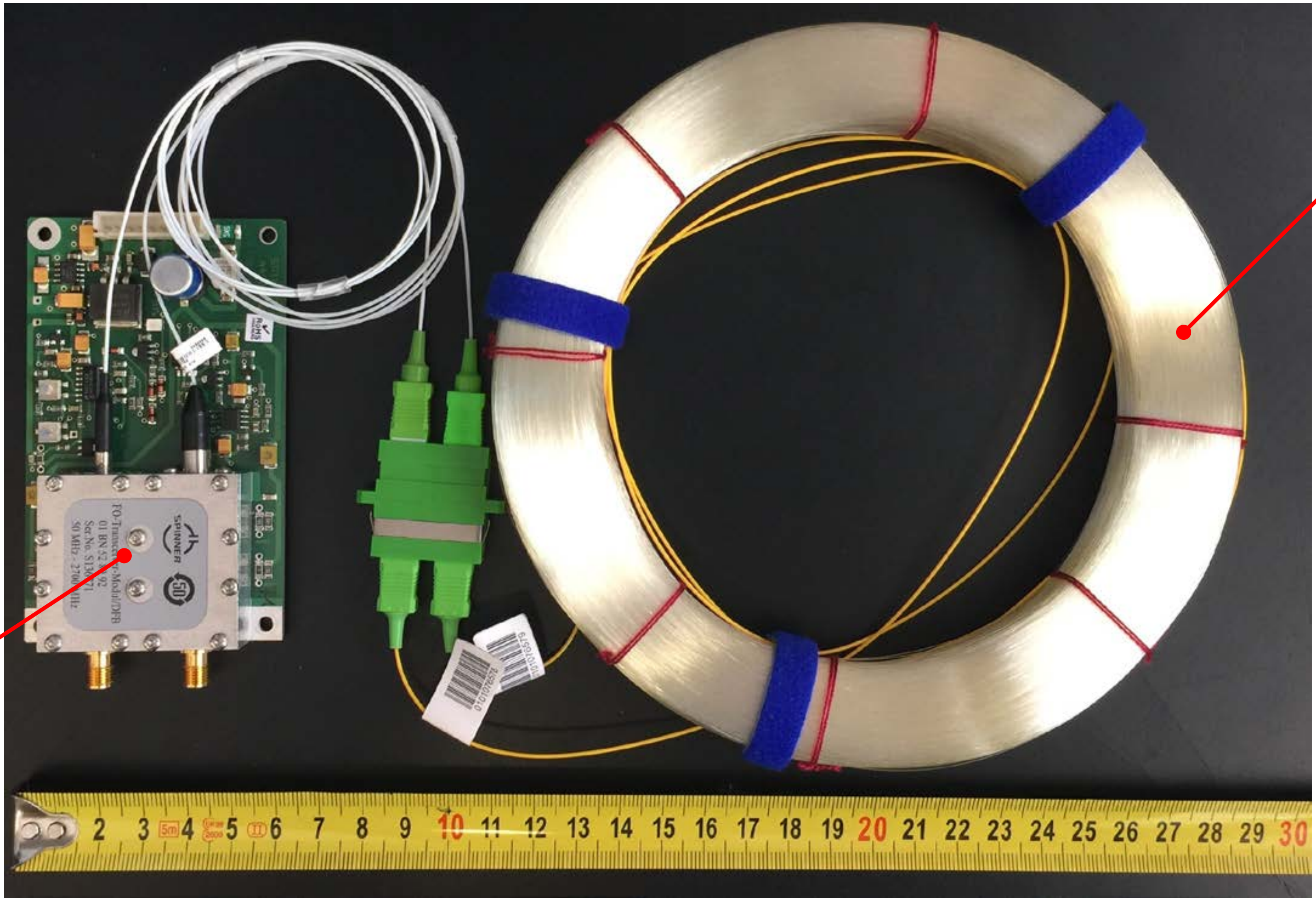
- SPS reference RF signals are generated in BA3
- SPS damper installed in BA2 (opposite direction than the beam is circulating)
- RF signals have to be made synchronous in BA2





How is the delay achieved

- Delays of several tens of μs can be easily obtained using single mode optical fibres with analogue optical transceivers

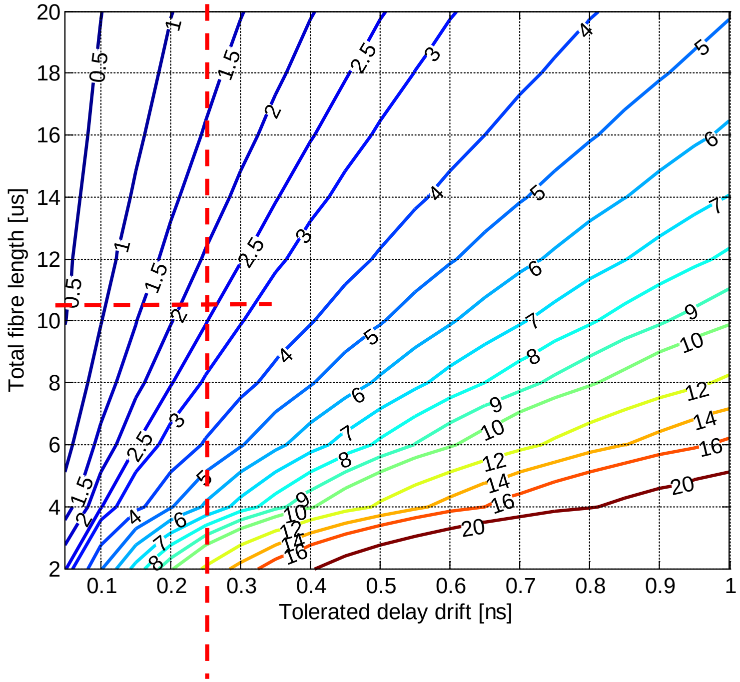


14.8 μs fiber coil (3 km)

Transceiver module

Status after summer 2015

- Thermal drift of optical fibre measured and characterized
- Prototype regulator designed and performance tested
- PCB design and mechanical parts drawings finalized, ready for production

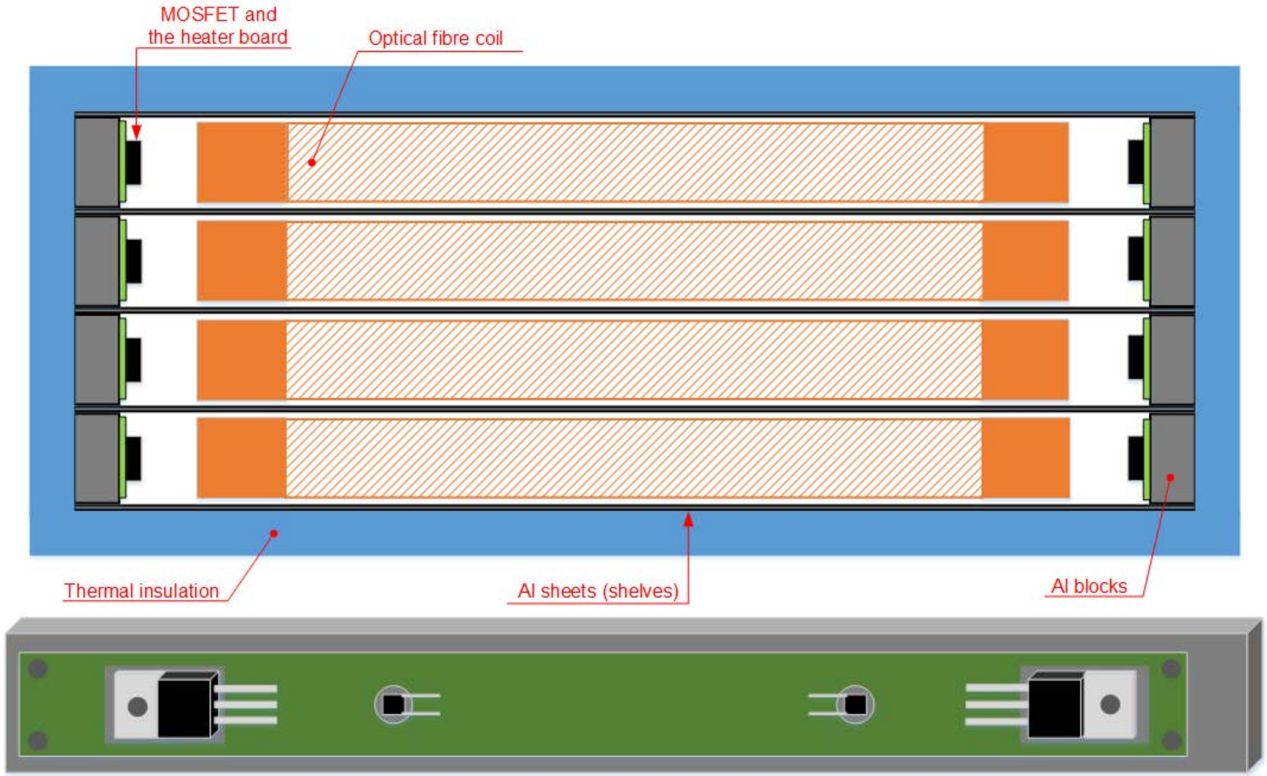


Maximum fibre temperature variation as a function of total fibre delay and tolerated delay drift.

Tolerated delay drift for correct damper operation is typically ±125 ps.

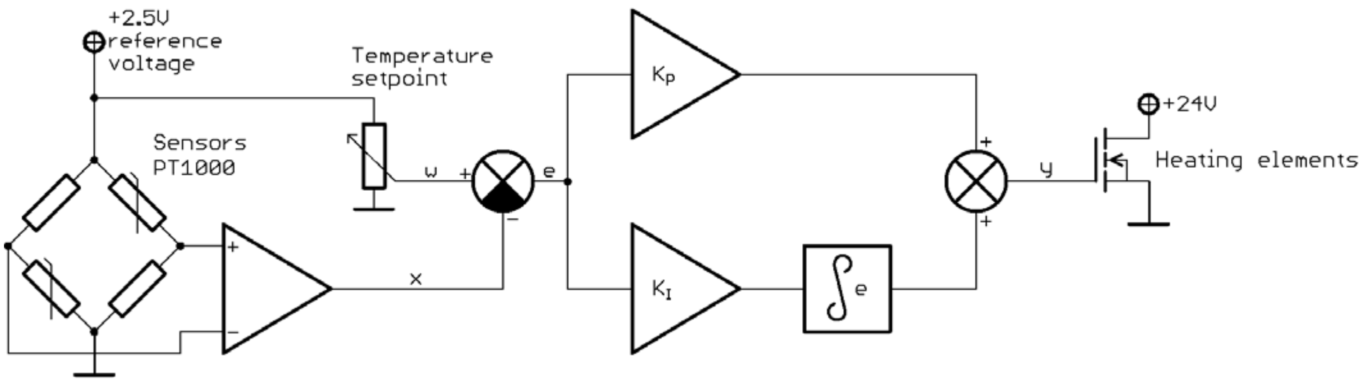
Design of thermally insulated enclosure

- Set-point temperature set above ambient, no need for active cooling
- Evenly spaced 8x heating MOSFET and 8x PT1000 temperature sensor
- Total available heating power of ~70 W

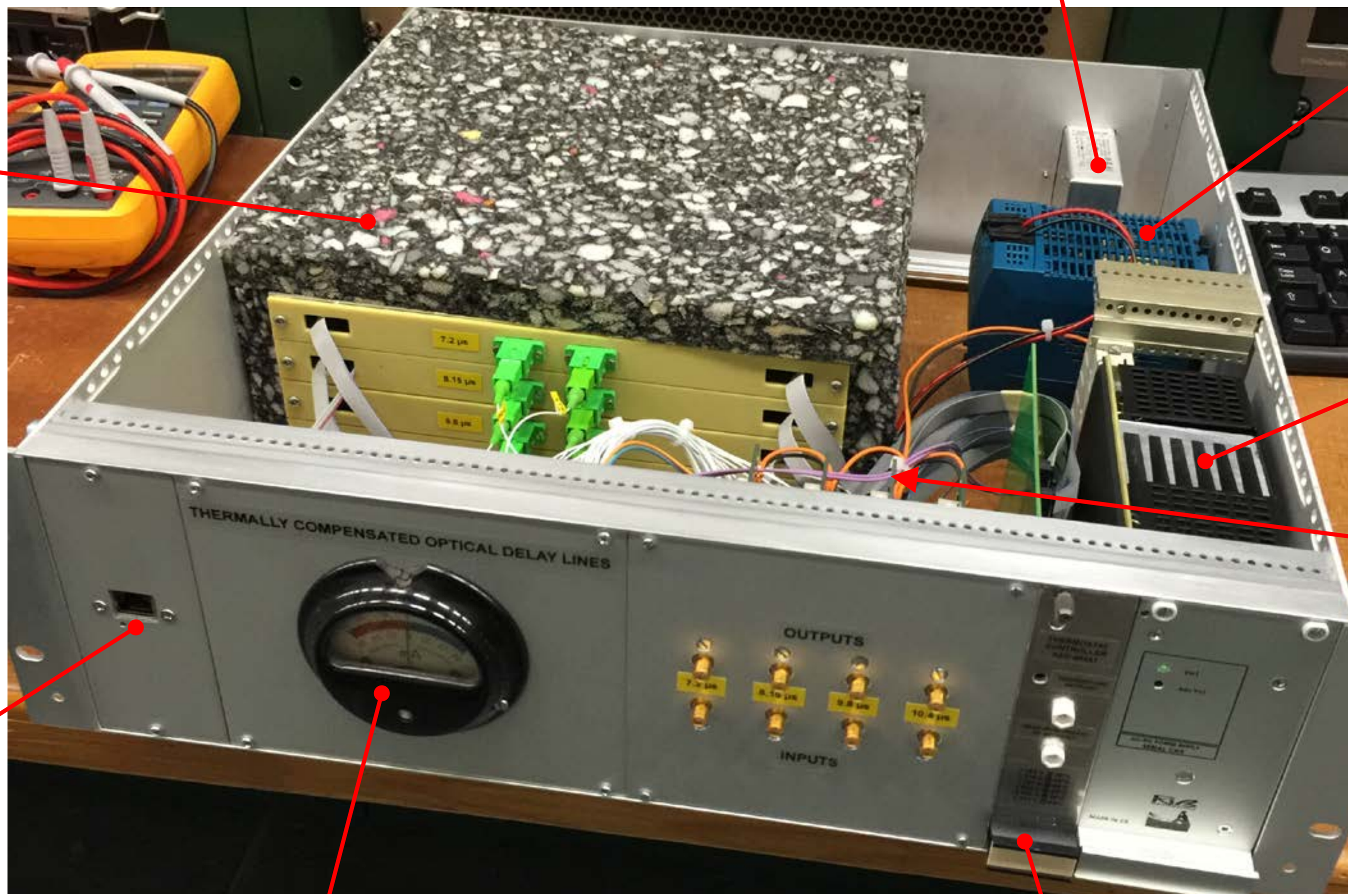


Design of regulator

- Fully analogue circuit
- PI topology
- Designed such that temperature induced drifts within the regulator are cancelling-out → very robust topology



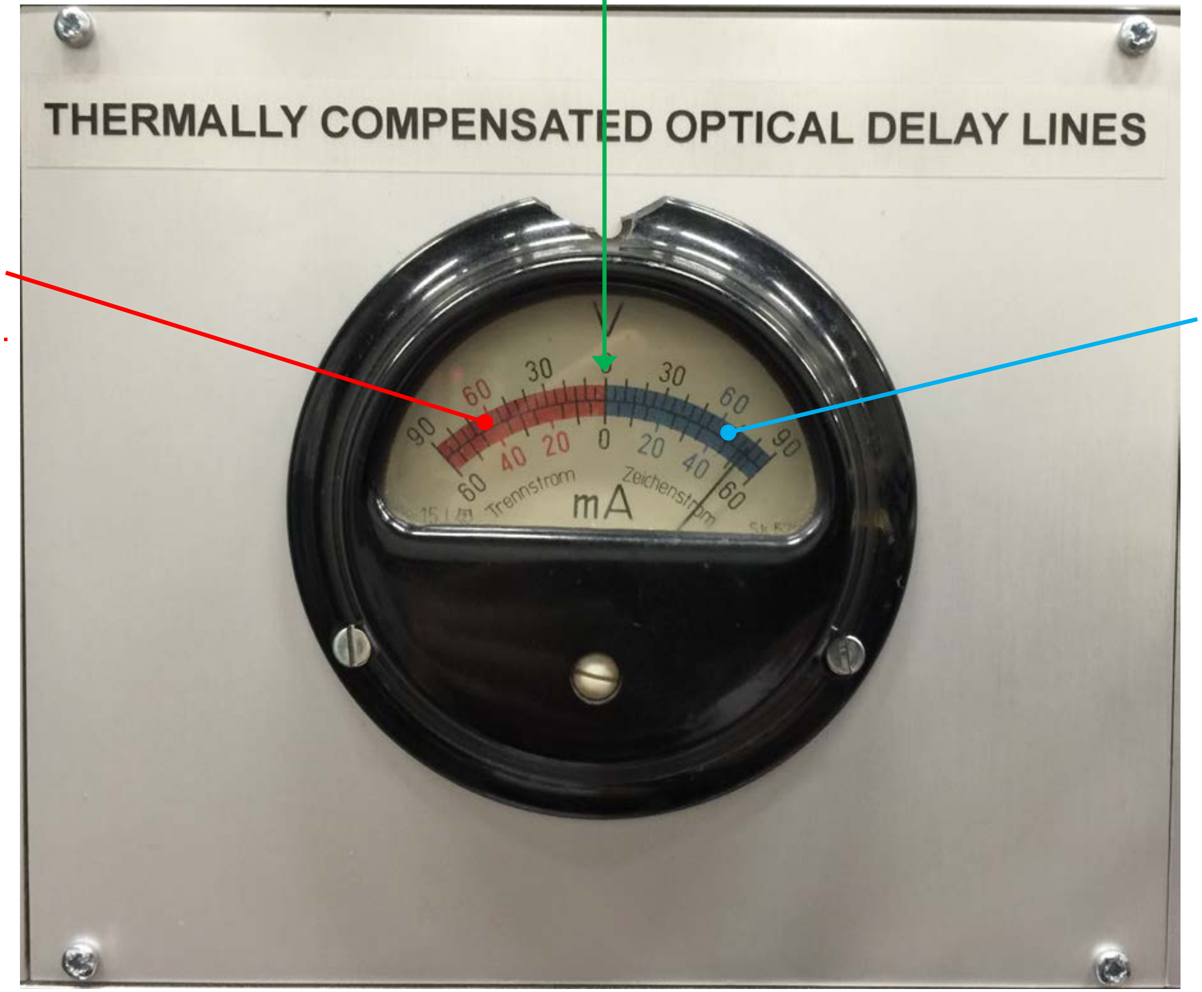
Fully assembled chassis (July 2016)



State of the regulator…

'**Sweet spot**' – set-point temperature reached

'**Hotter**' than set-point temperature. Should never reach this state under normal operation.



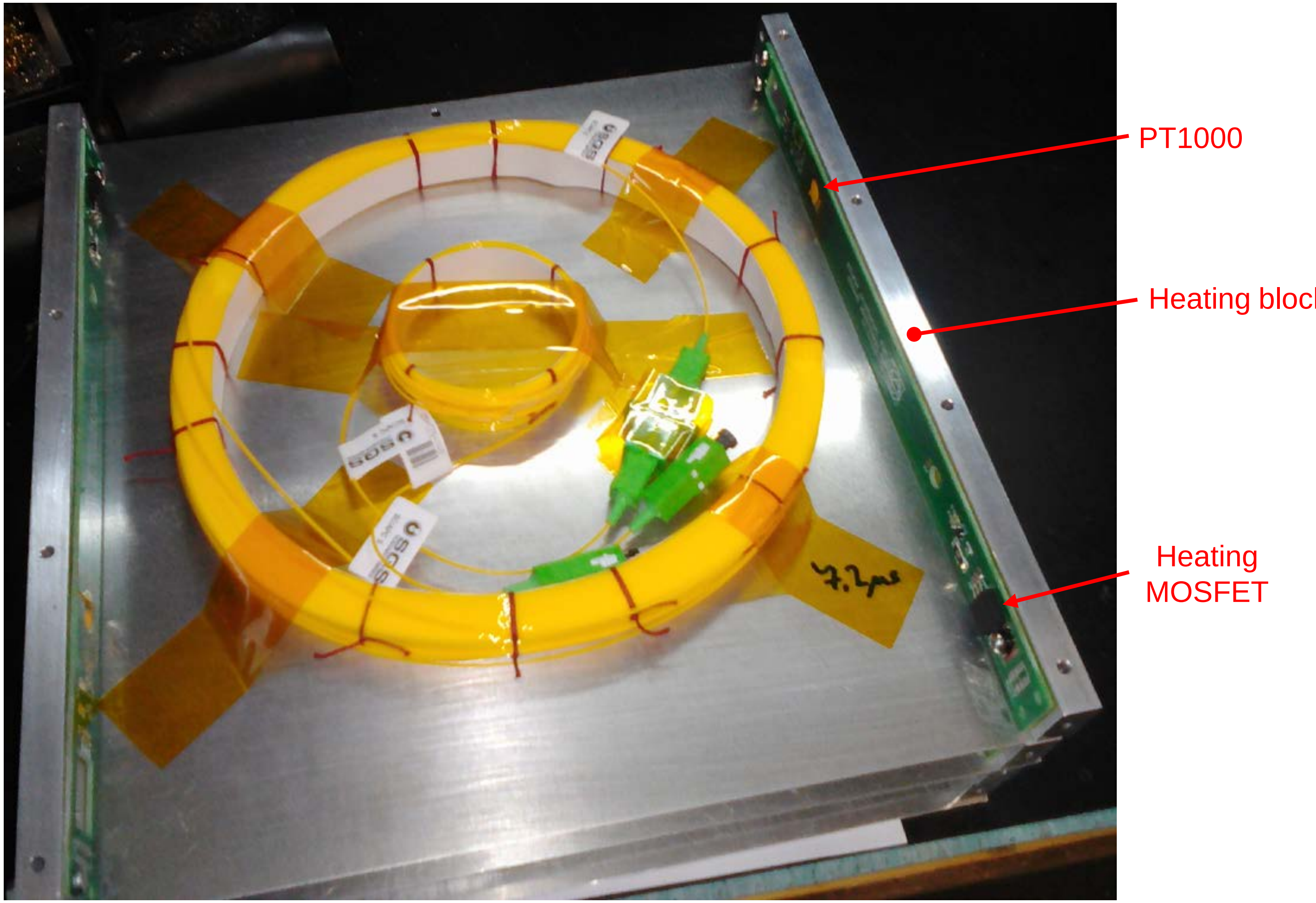
'**Colder**' than set-point temperature. Deviation during the initial warm-up.

Detail of optical fiber

- Fiber is split in two, for precise trimming of total electrical length

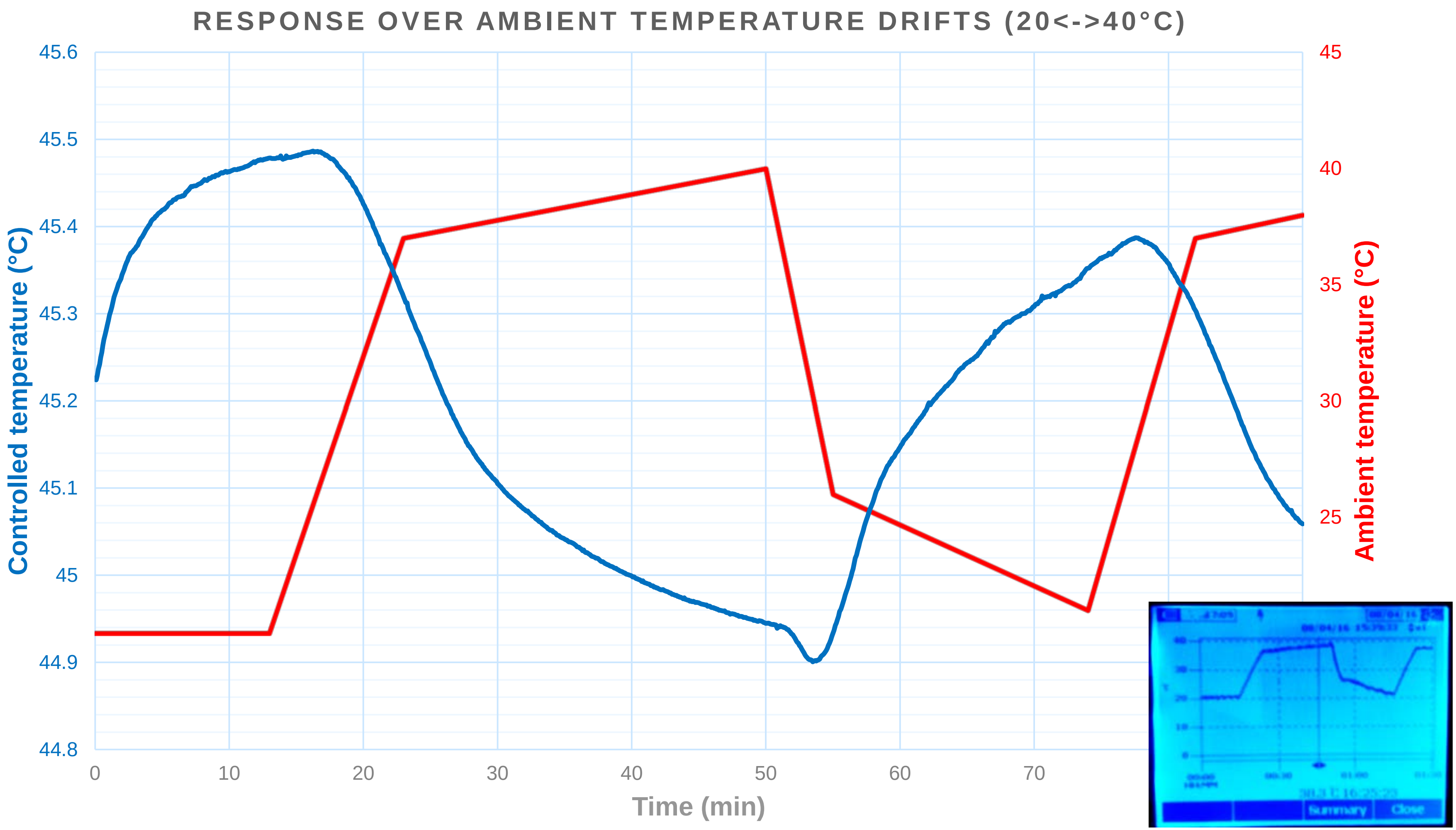
Configuration of fibers:

7.2 µs	=	6.7 µs	+	0.5 µs
8.15 µs	=	7.65 µs	+	0.5 µs
9.8 µs	=	9.3 µs	+	0.5 µs
10.4 µs	=	9.9 µs	+	0.5 µs



Regulator performance test

- Entire chassis was put into thermal chamber, 20°C step in ambient temp.

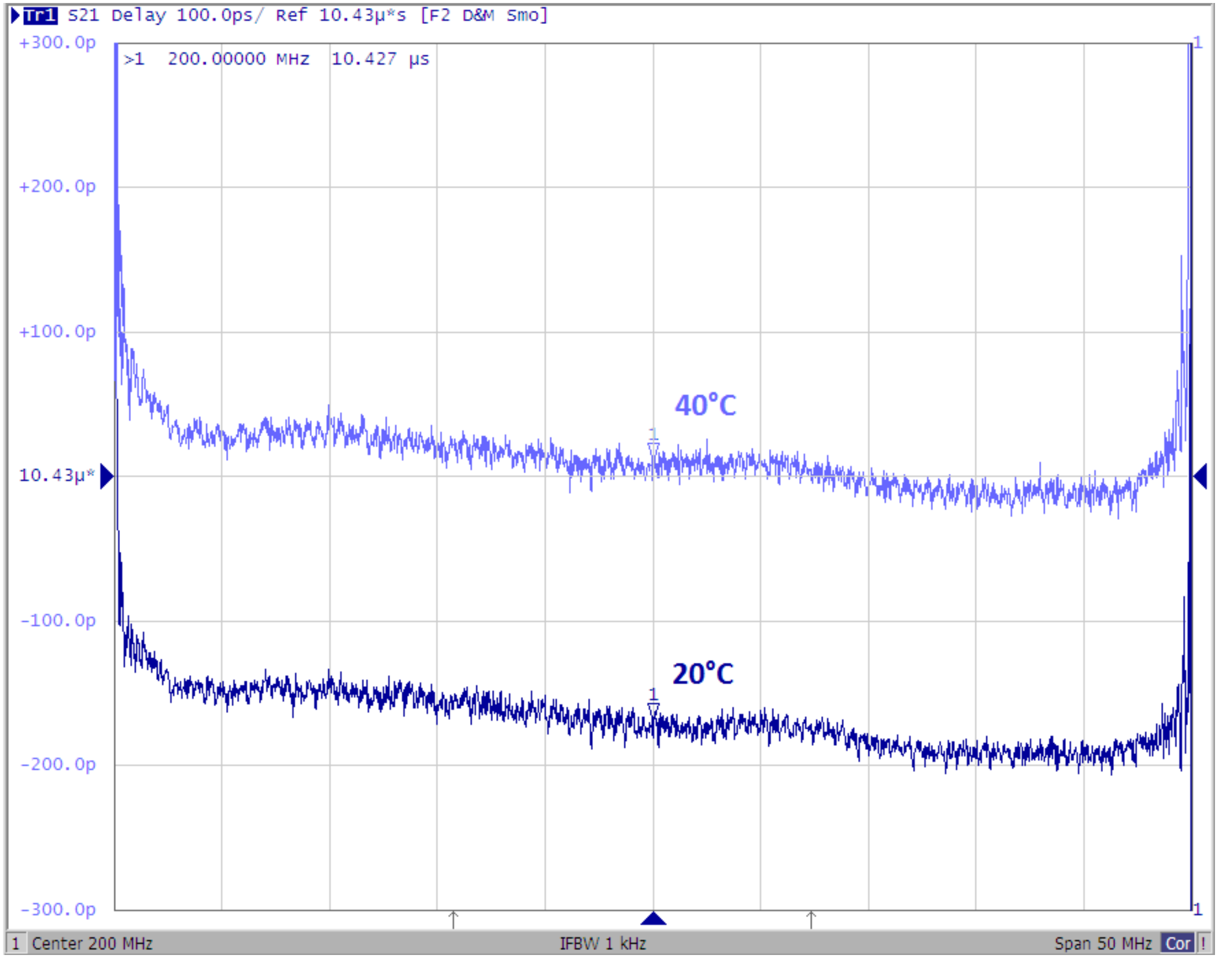


Electrical delay stability

- Group delay of the longest (10.4 µs) fiber

- Only 200 ps drift over 20 °C step in ambient temperature

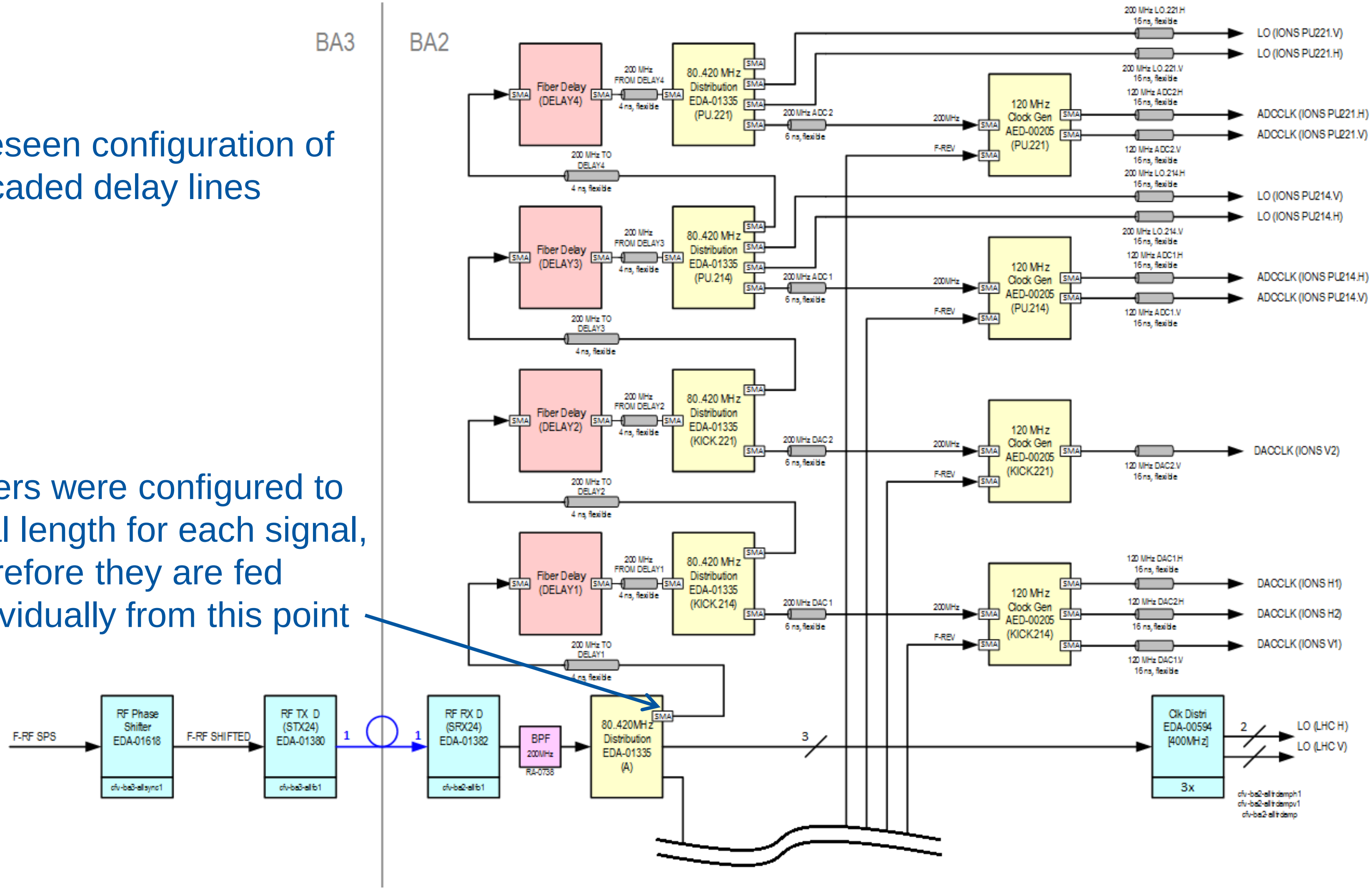
- Both traces were captured after several hours



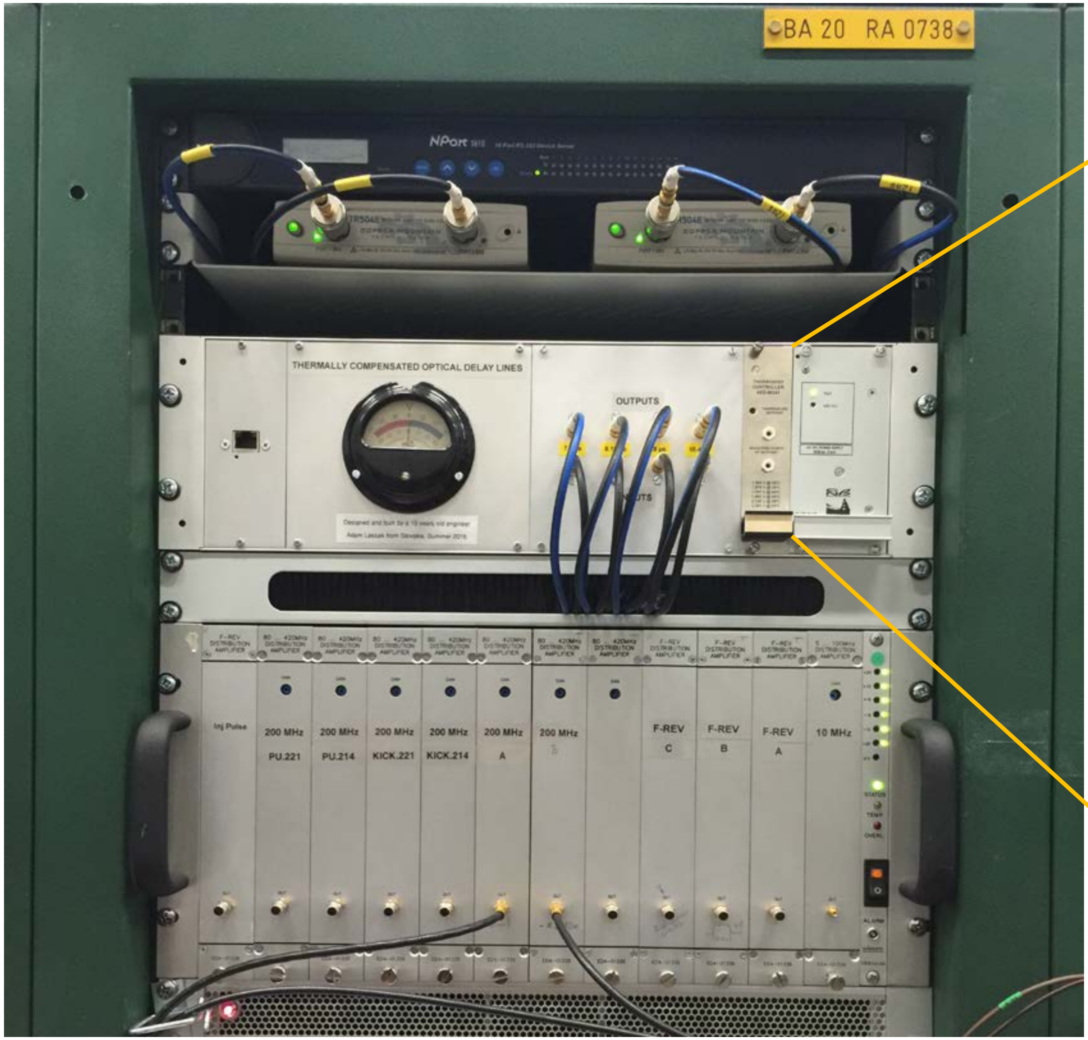
Installation in BA2

Foreseen configuration of cascaded delay lines

Fibers were configured to total length for each signal, therefore they are fed individually from this point

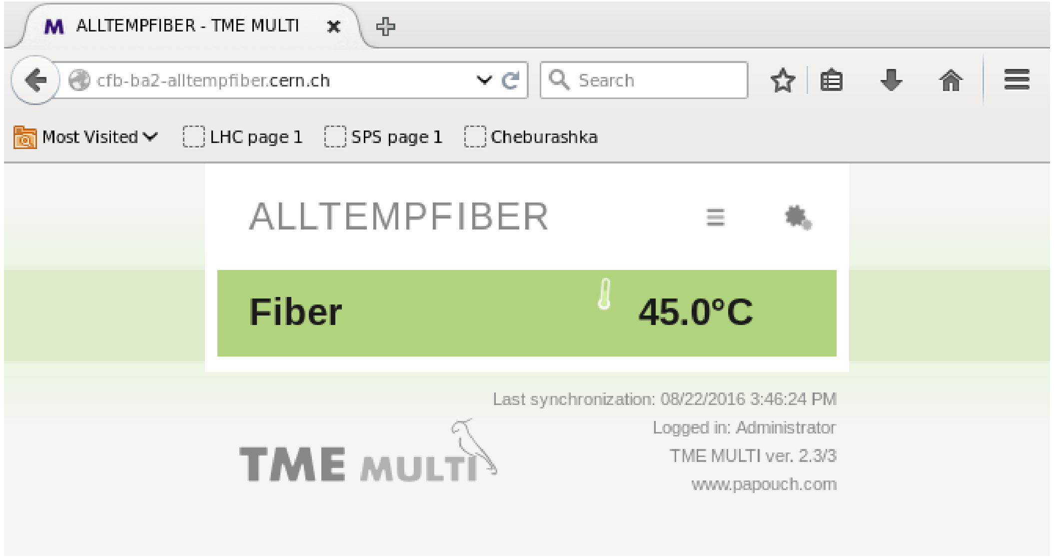


Chassis installed in BA2



Performance under real conditions

- Chassis was installed in BA2 on 10. August 2016
- Measured ambient temperature in BA2 varying between 22°C and 29°C
- First tests with ion beam revealed that the achieved total fiber delay for the two pick-ups is well within tolerable limits
- Fiber temperature level was found to be constant at 45°C since instalment

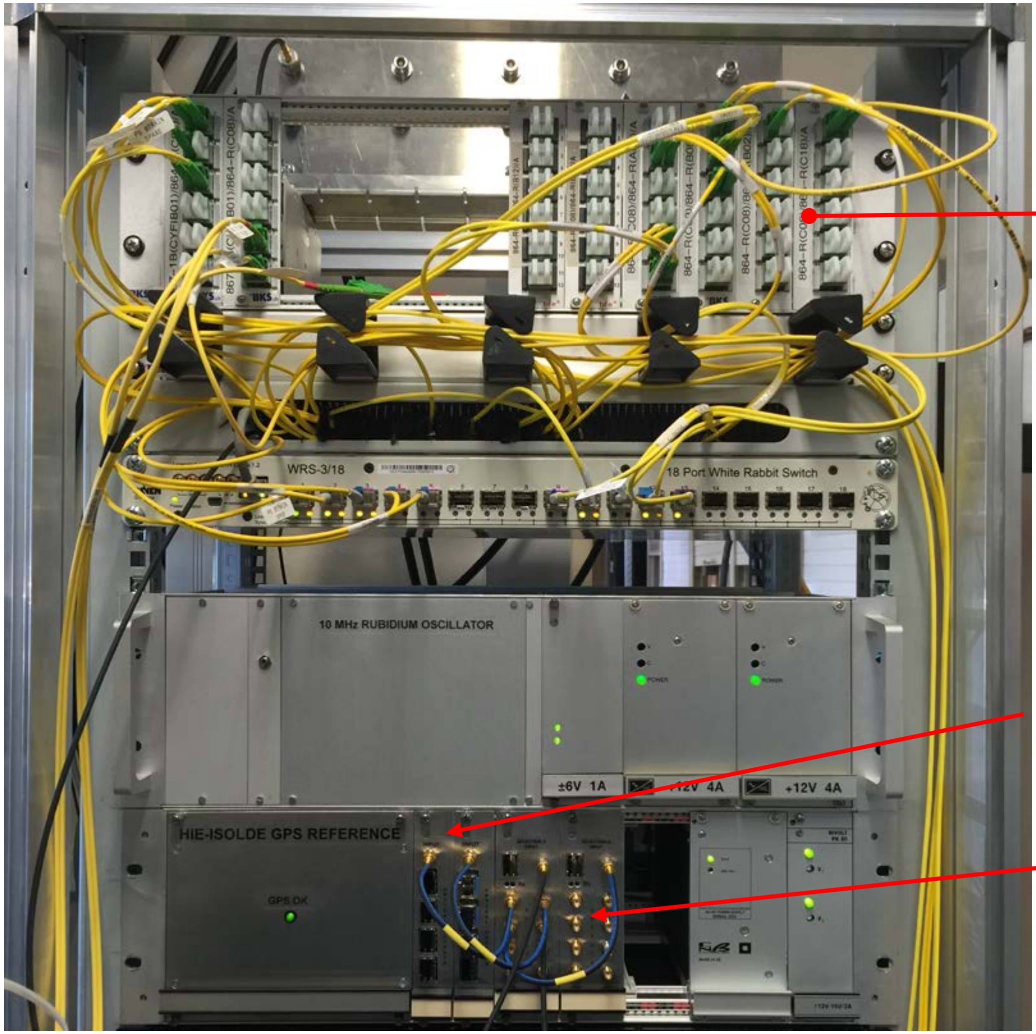


Other projects I was working on during my stay

- Reference Signal Distribution in LLRF Labs
- SPS Damper Pickup and Test Point Signal Fan-out

Reference Signal Distribution in LLRF Labs

- A spare HIE-Isolde GPS reference is running in the lab
- A 2nd hand rubidium oscillator is running in the lab
- 864-R-C08 is a fiber starpoint with connections to all LLRF labs
- …10MHz reference anyone?



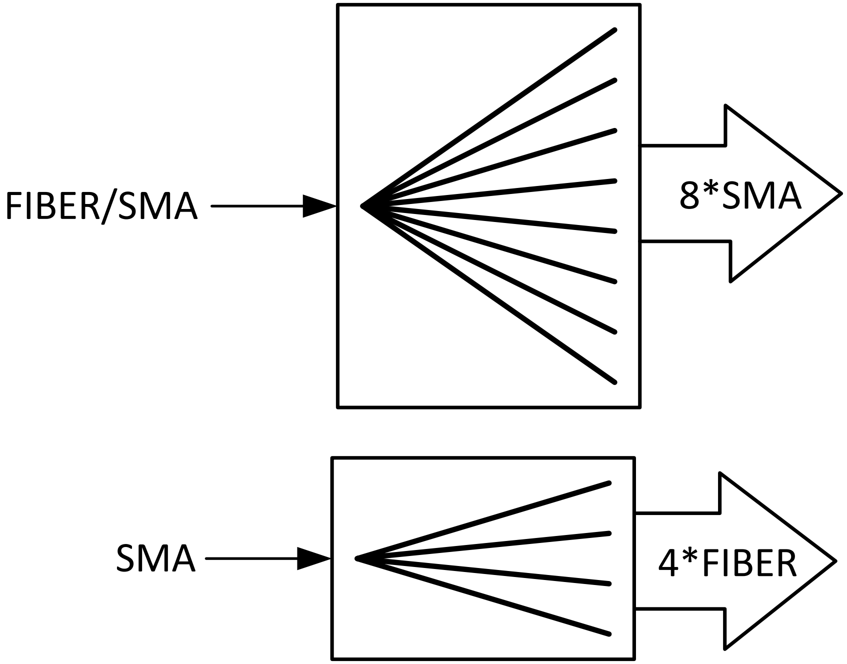
Sockets for labs distribution

Optical outputs for between labs distribution

SMA outputs for local distribution

Reference Signal Distribution in LLRF Labs

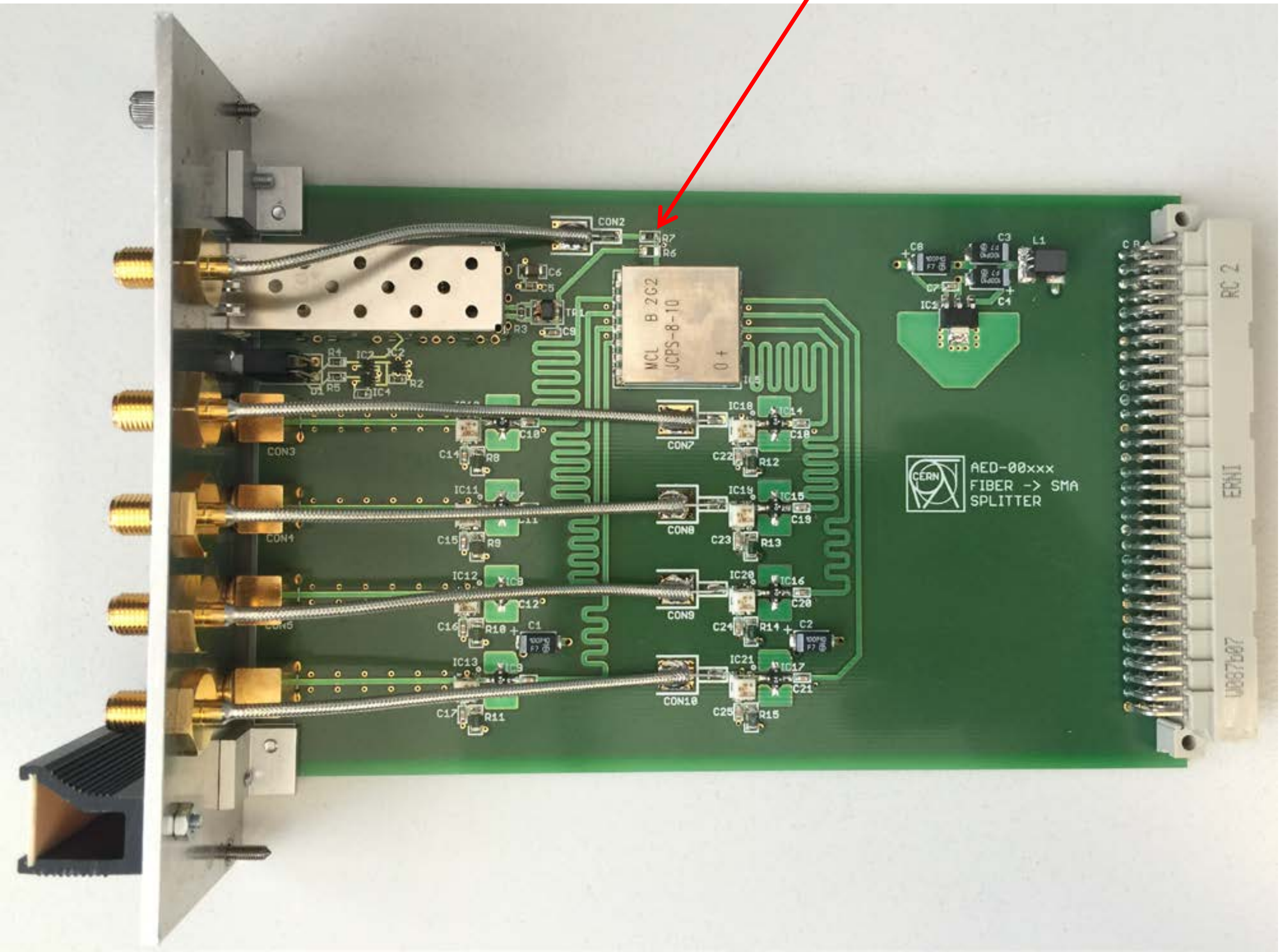
- Two designs; Fiber to SMA distributor and SMA to Fiber distributor
- BW ~ 5 MHz to 1 GHz
- Single rail power supply 6 V, ~0.5 A per board
- Based on Finisar FTLF1321 transceiver modules



SMA distributor board

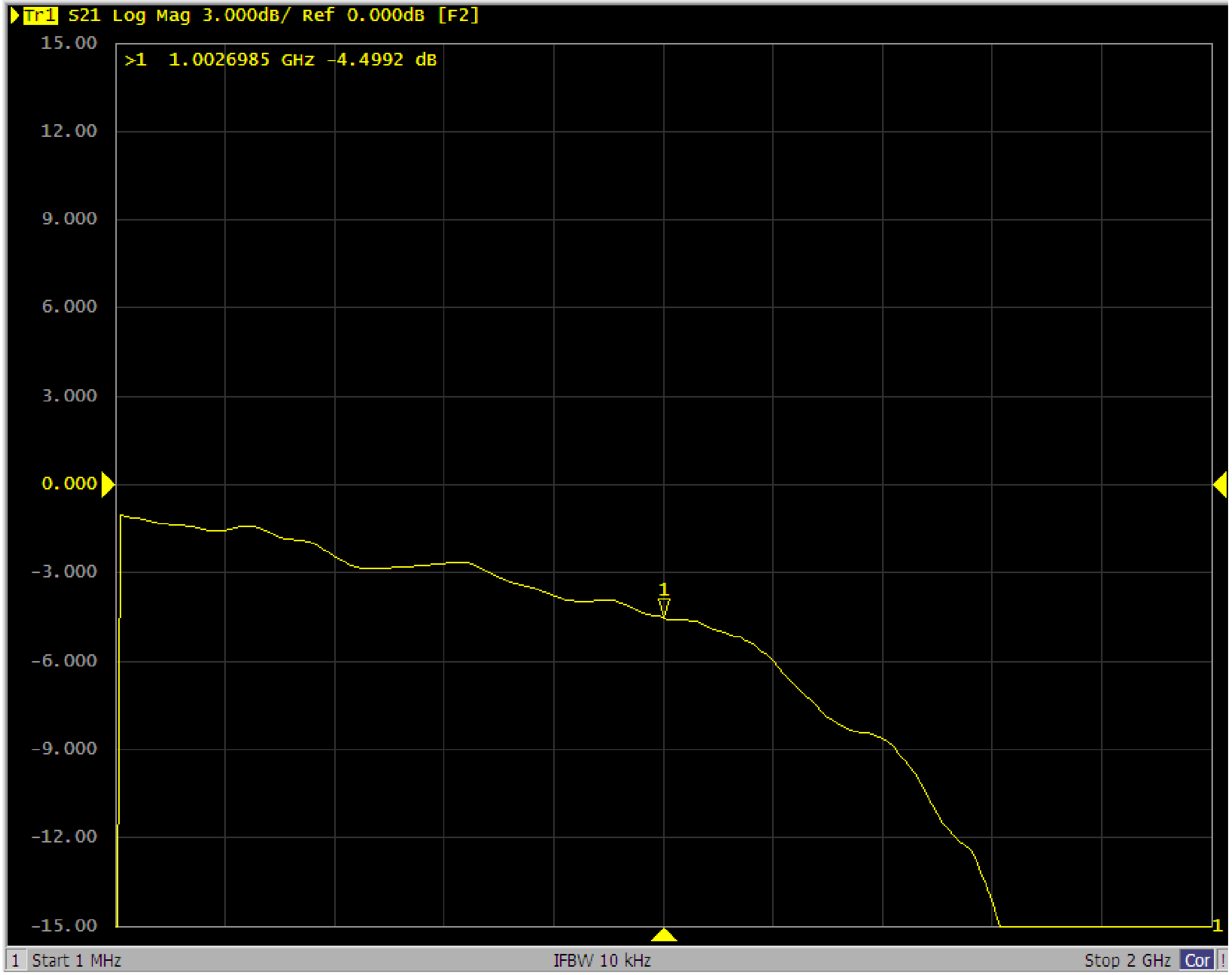
- 1x Fiber/SMA input to 8x SMA output

0 Ω resistor to select between inputs



Frequency response of Fiber to SMA distributor

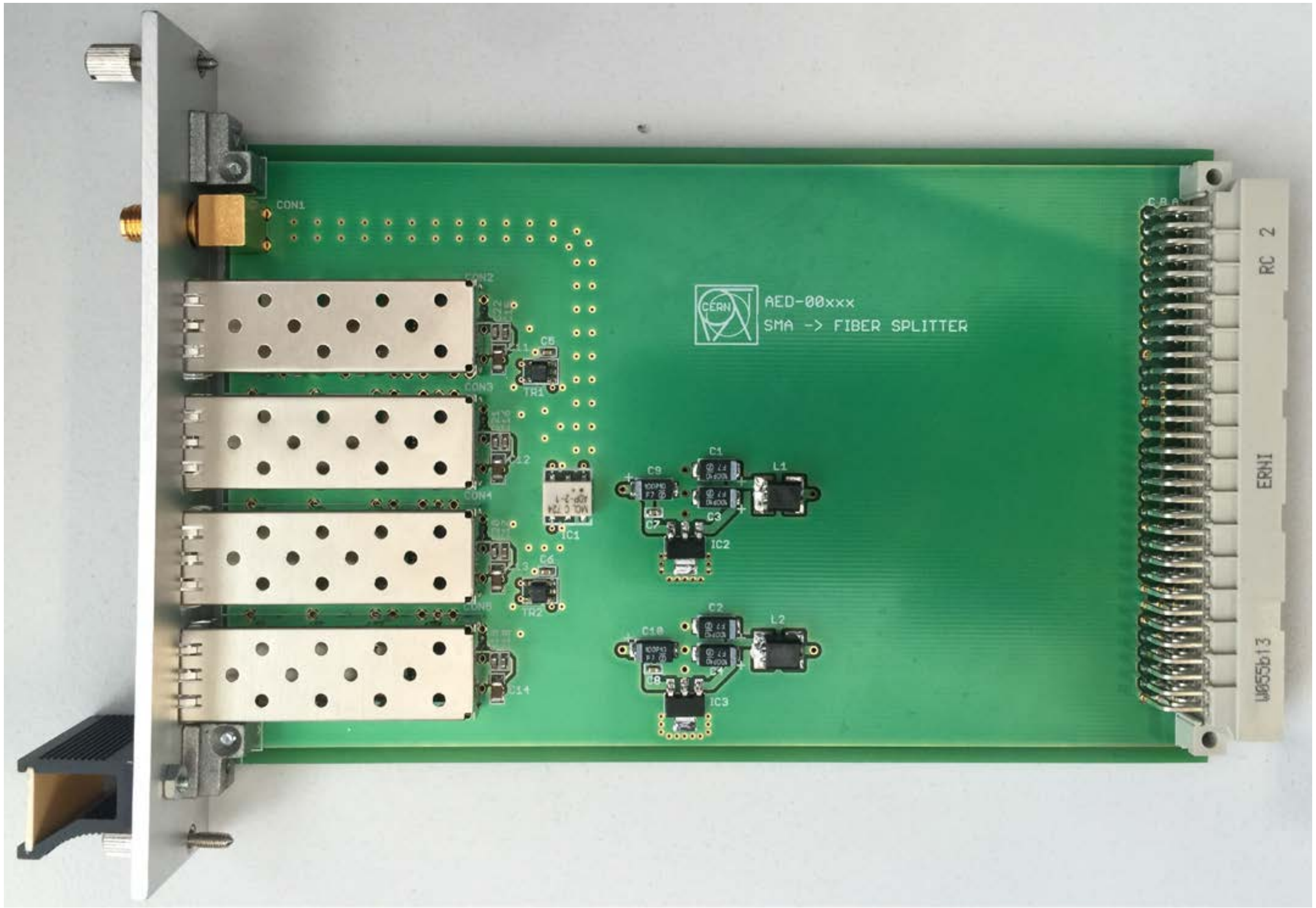
Gain vs. Frequency -3 dB @ 1 GHz



*SMA input was used for this measurement

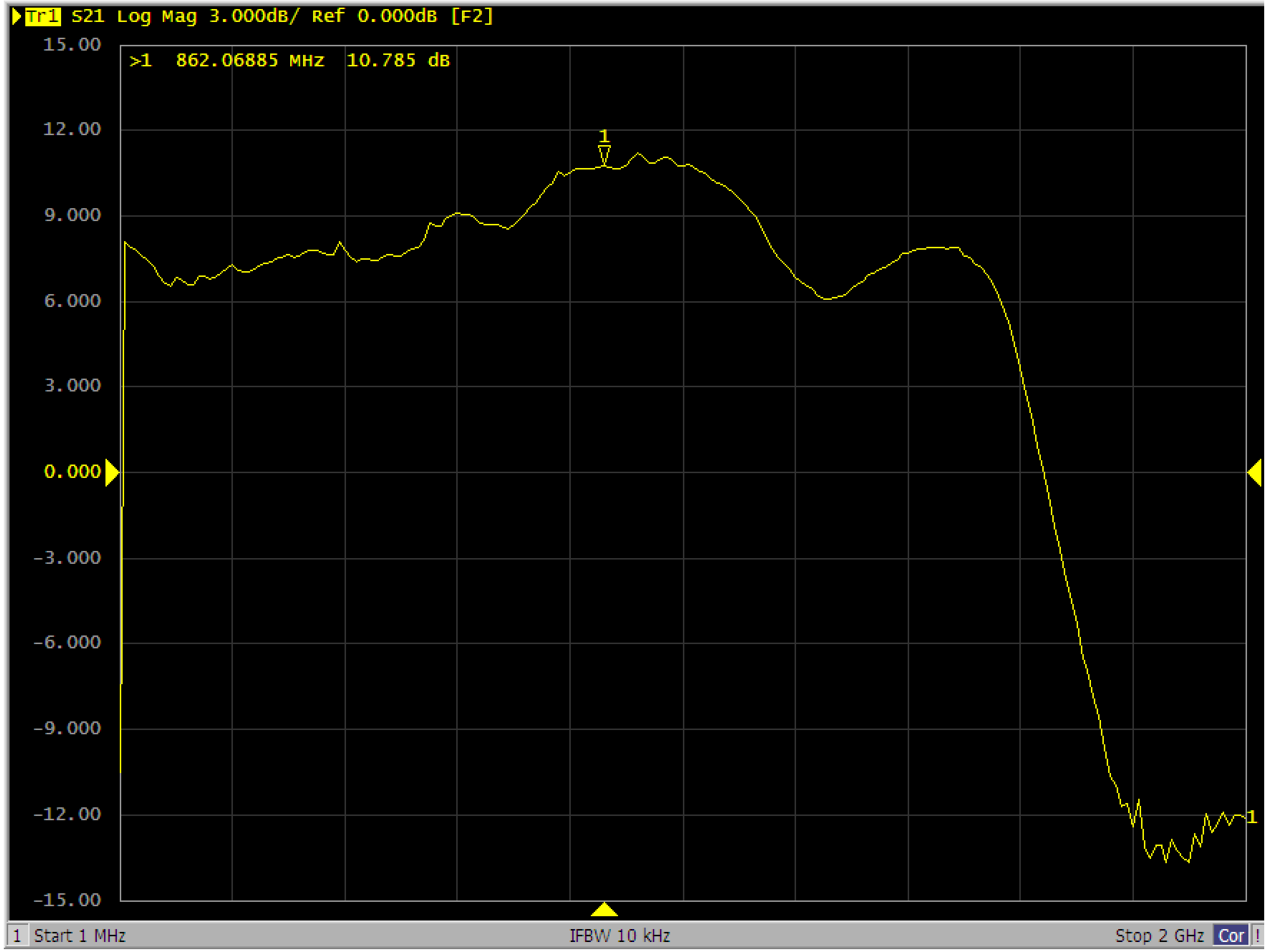
Fiber distributor board

- 1x SMA input to 4x Fiber output



Frequency response of SMA to Fiber distributor

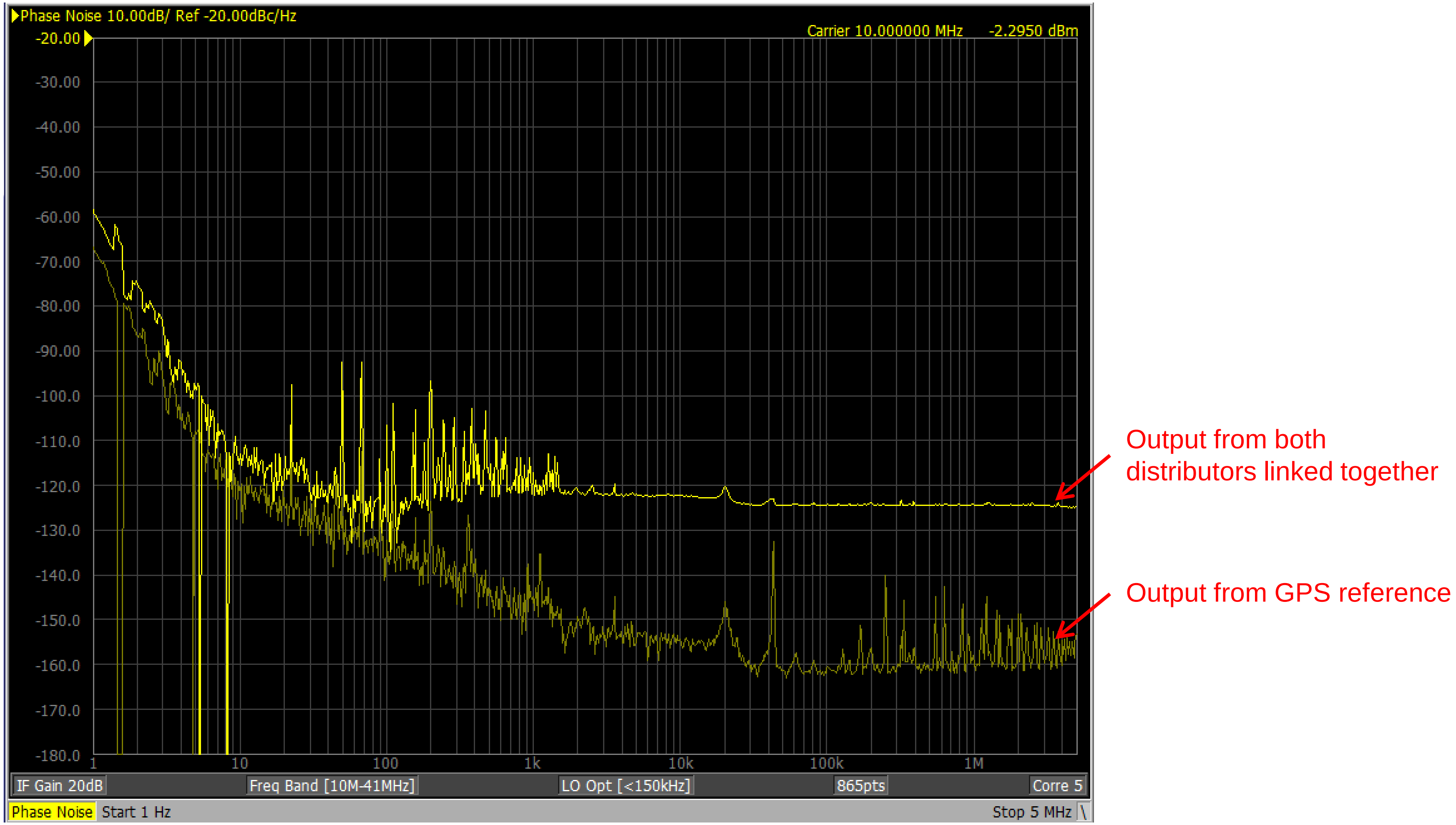
Gain vs. Frequency   -3 dB @ 850 MHz



*Both distributors were linked together for this measurement

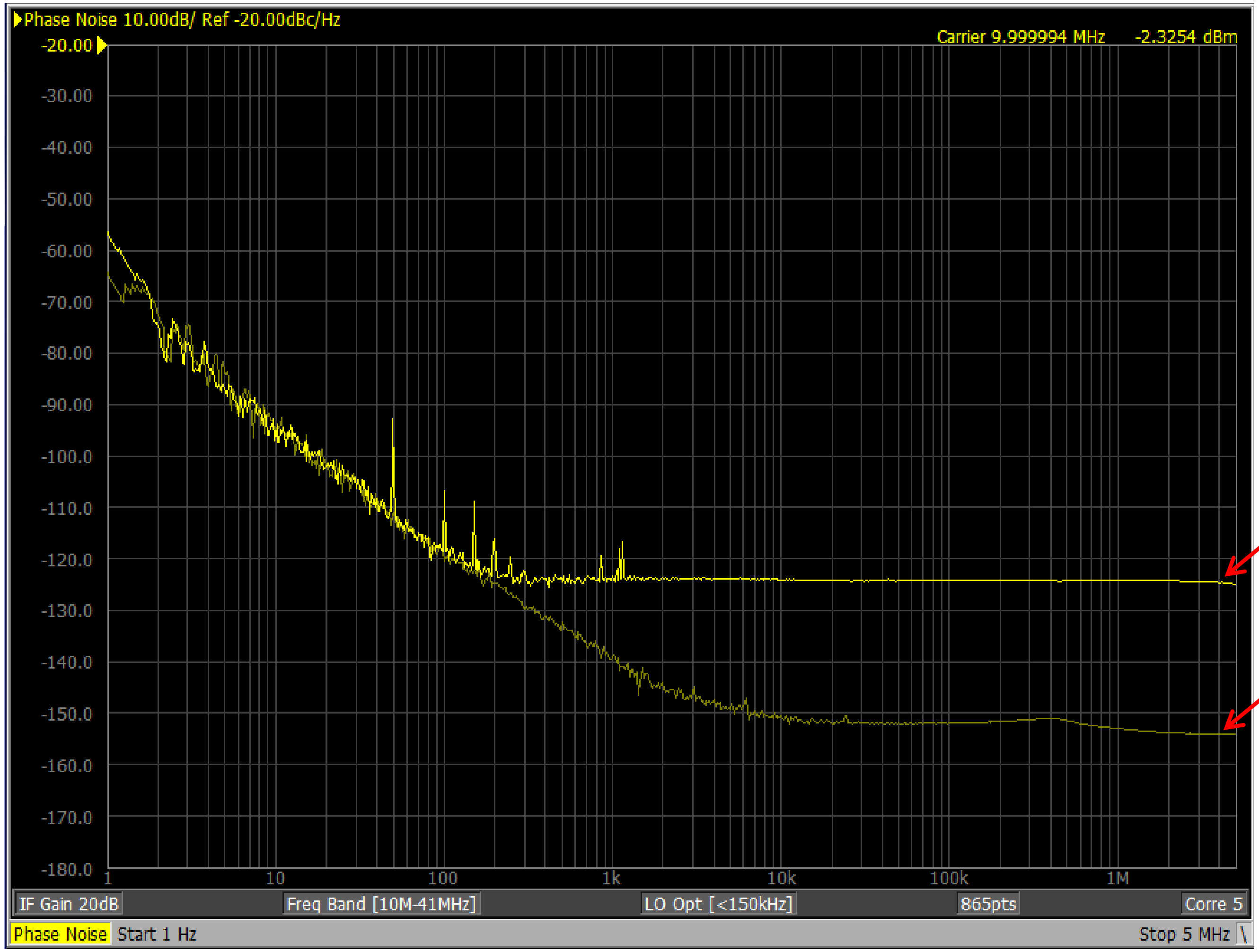
Phase noise measurement

- HIE-ISOLDE GPS Reference as source of 10 MHz



Phase noise measurement

- Signal generator SMC100A as source of 10 MHz

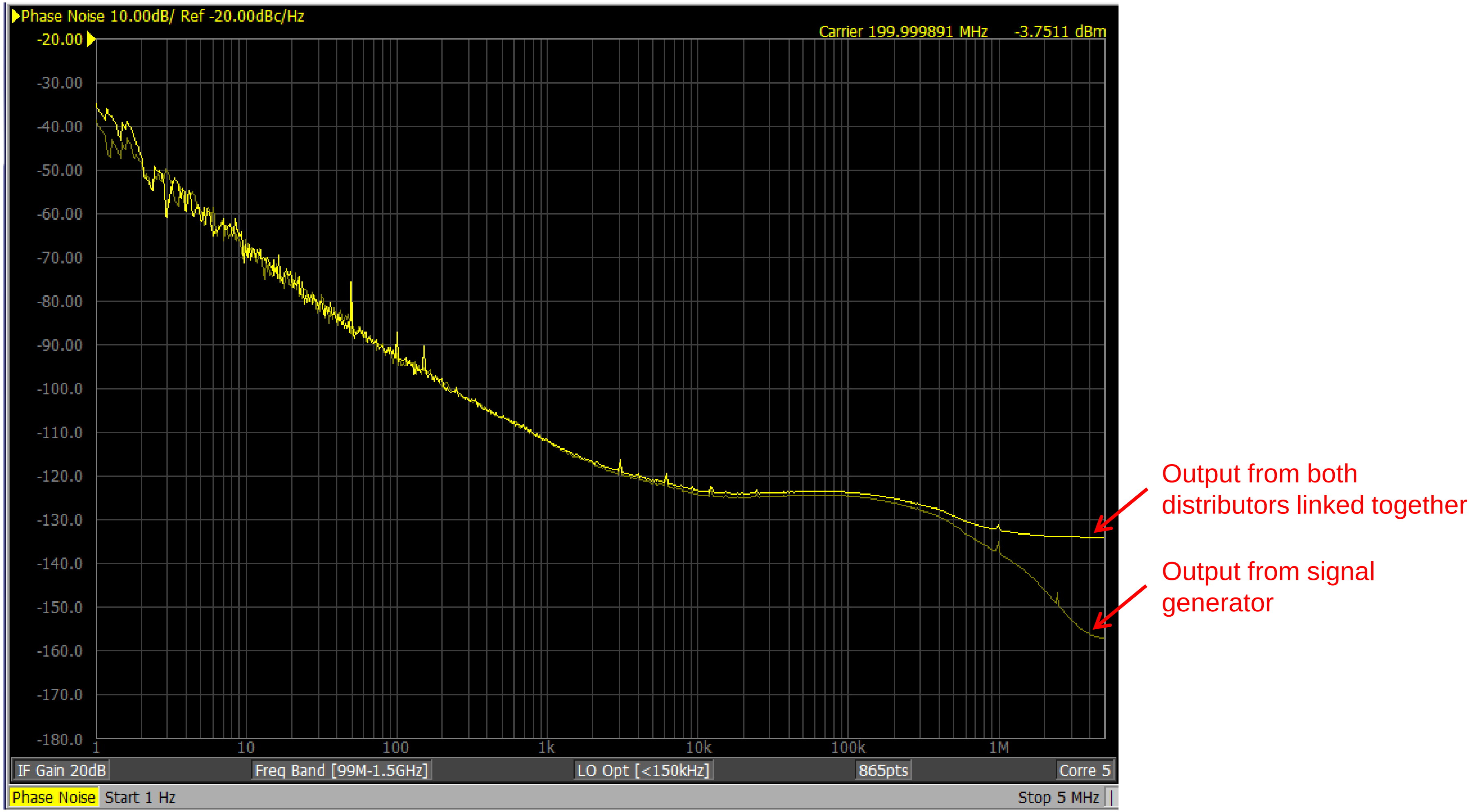


Output from both distributors linked together

Output from signal generator

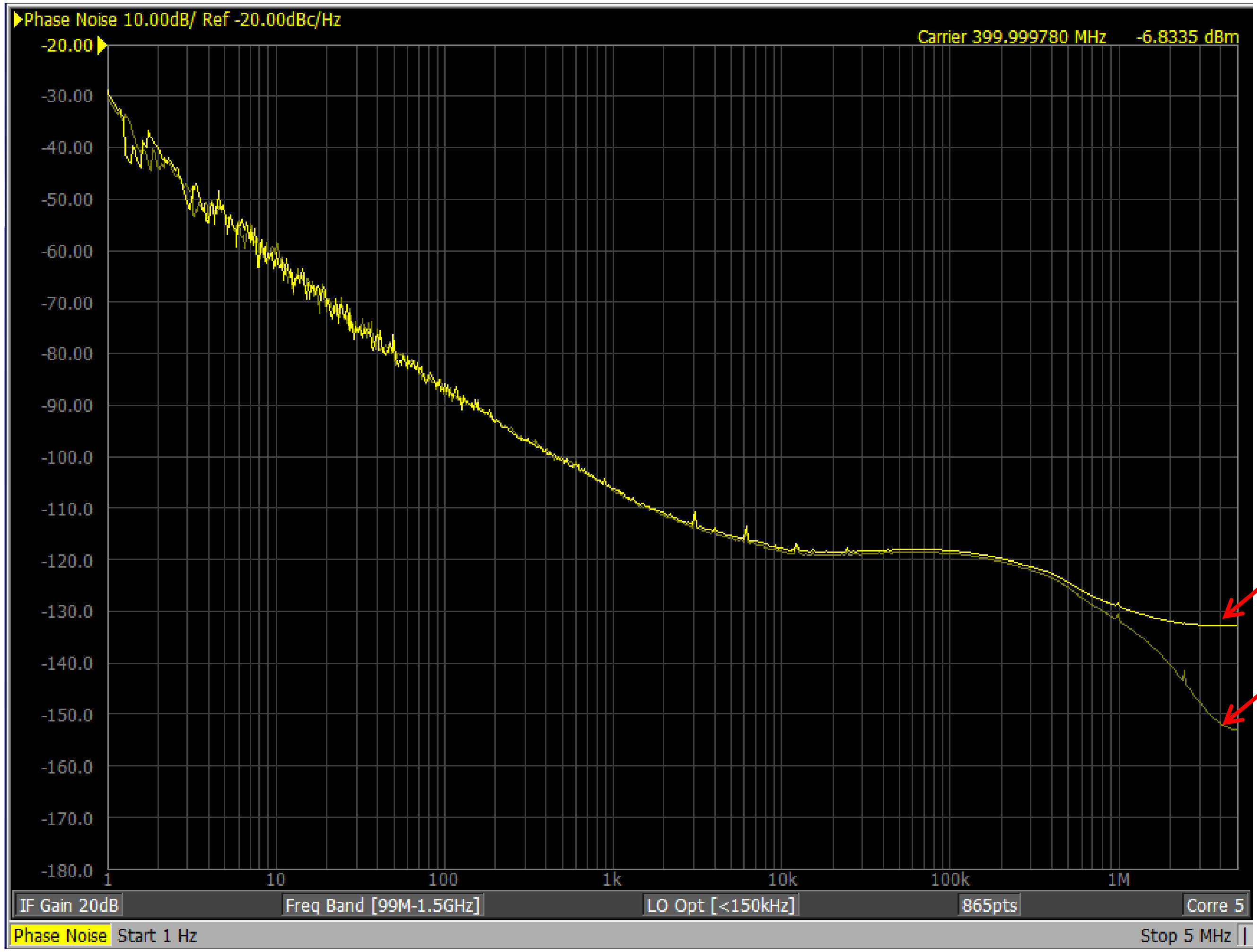
Phase noise measurement

- Signal generator SMC100A as source of 200 MHz



Phase noise measurement

- Signal generator SMC100A as source of 400 MHz

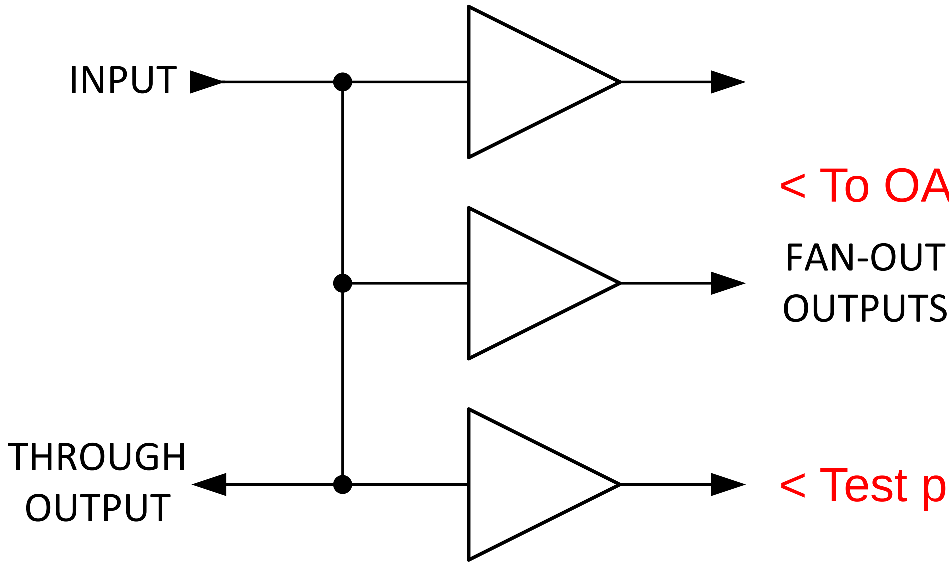


Output from both distributors linked together

Output from signal generator

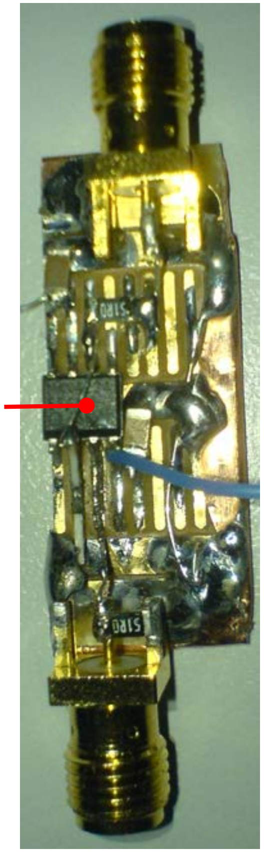
SPS Damper Pickup and Test Point Signal Fan-out

- BW < 250 MHz
- 50 Ω input/output characteristic impedance
- Signal level max. 10 dBm
- Gain 0 dB
- Full BW on through output for switching matrix

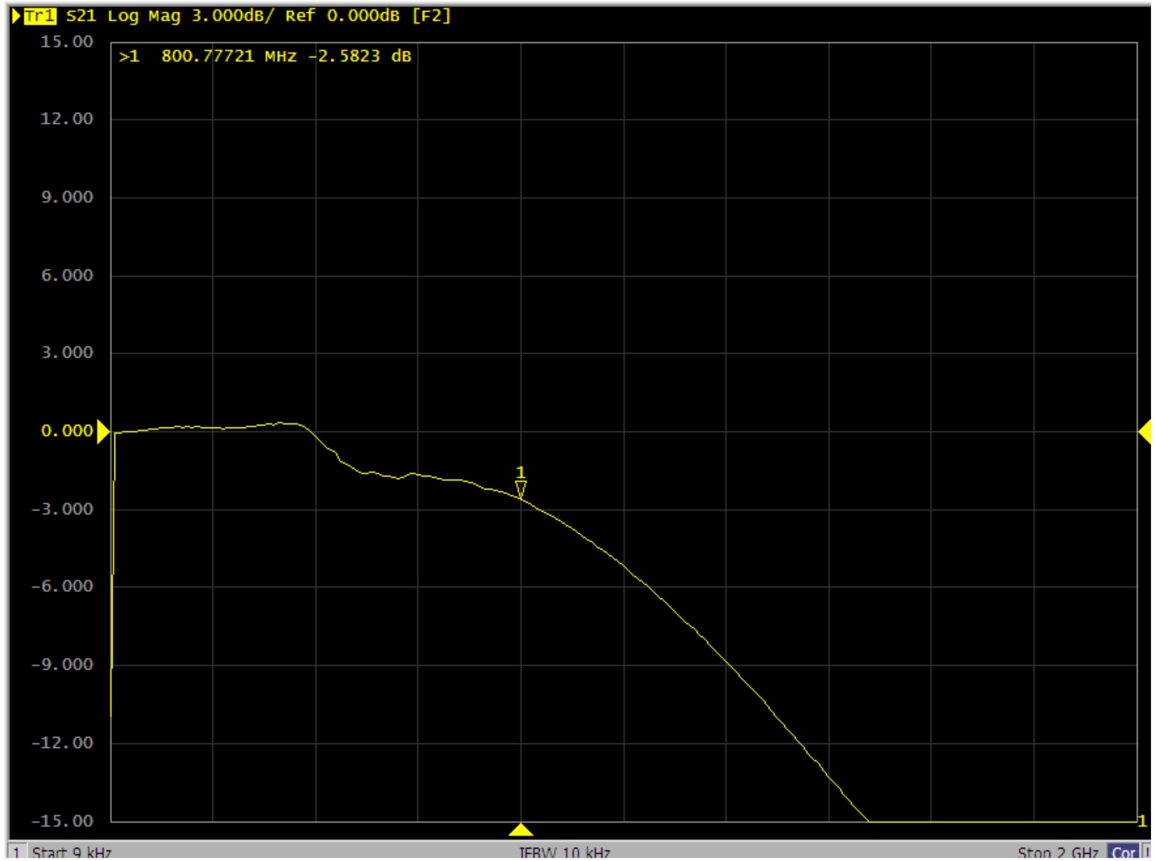


Frequency response of test circuit

MAX4224

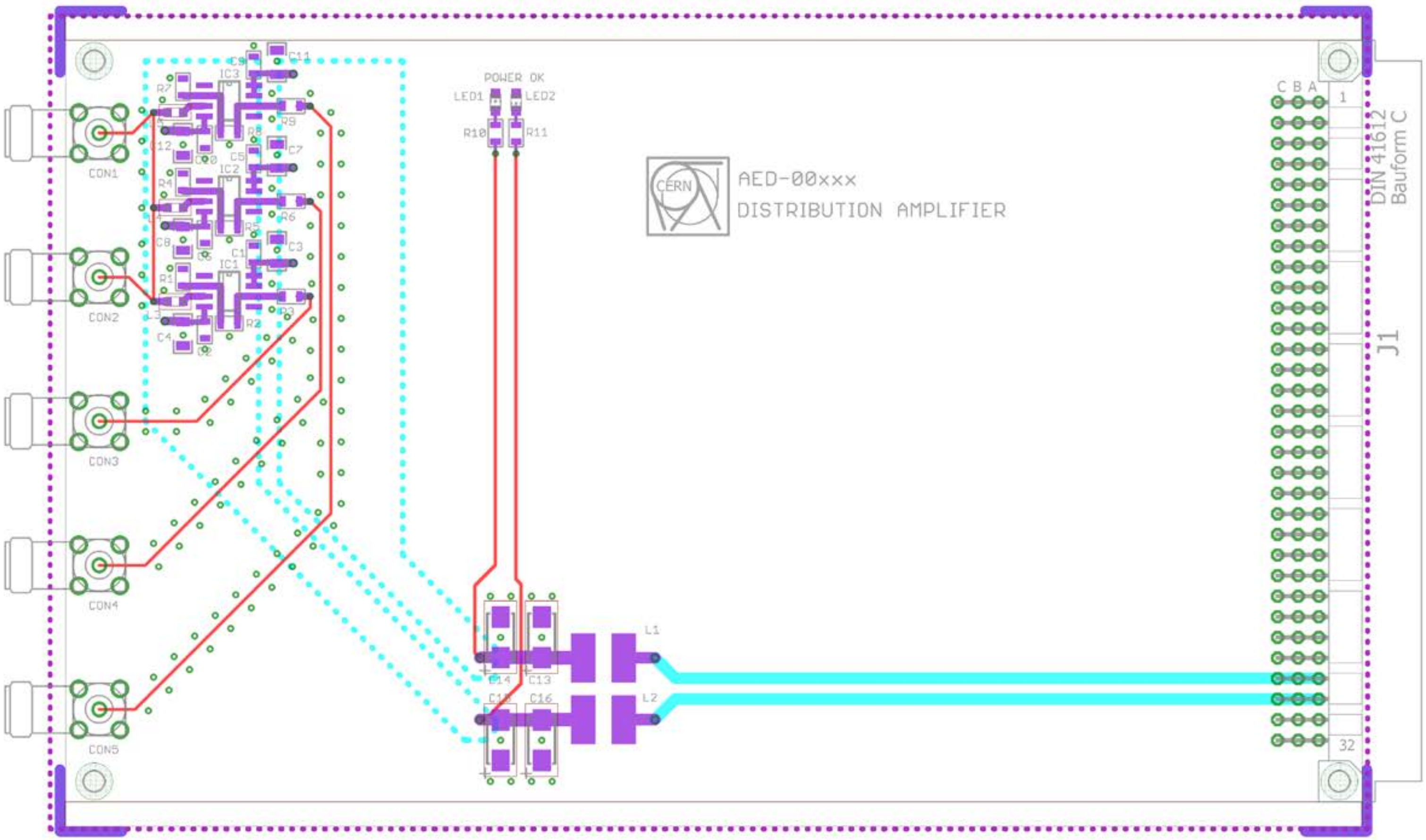


Gain vs. Frequency -3 dB @ 800 MHz; input power 10 dBm



SPS Damper Pickup and Test Point Signal Fan-out

- Prototype PCB sent for production



Questions?

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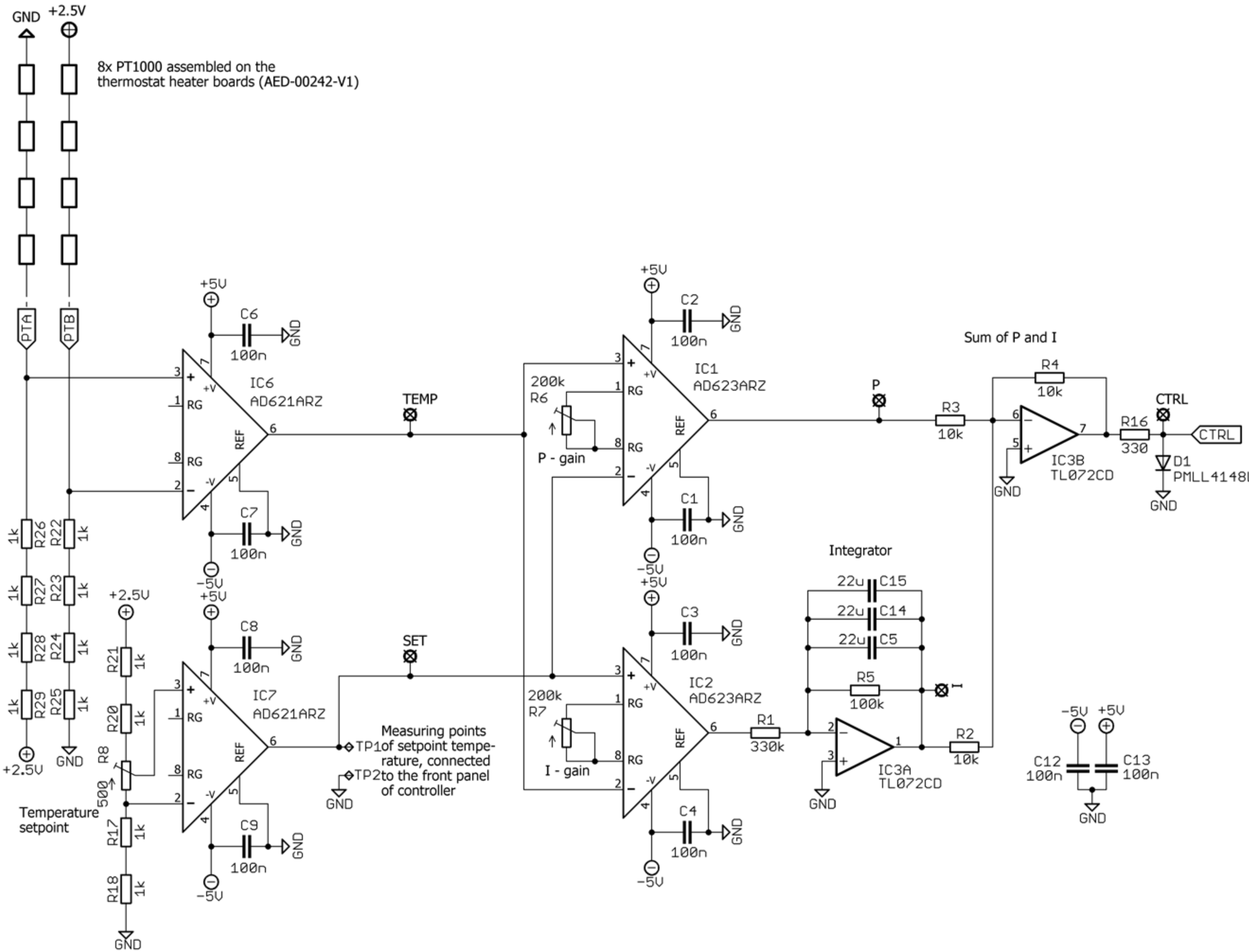
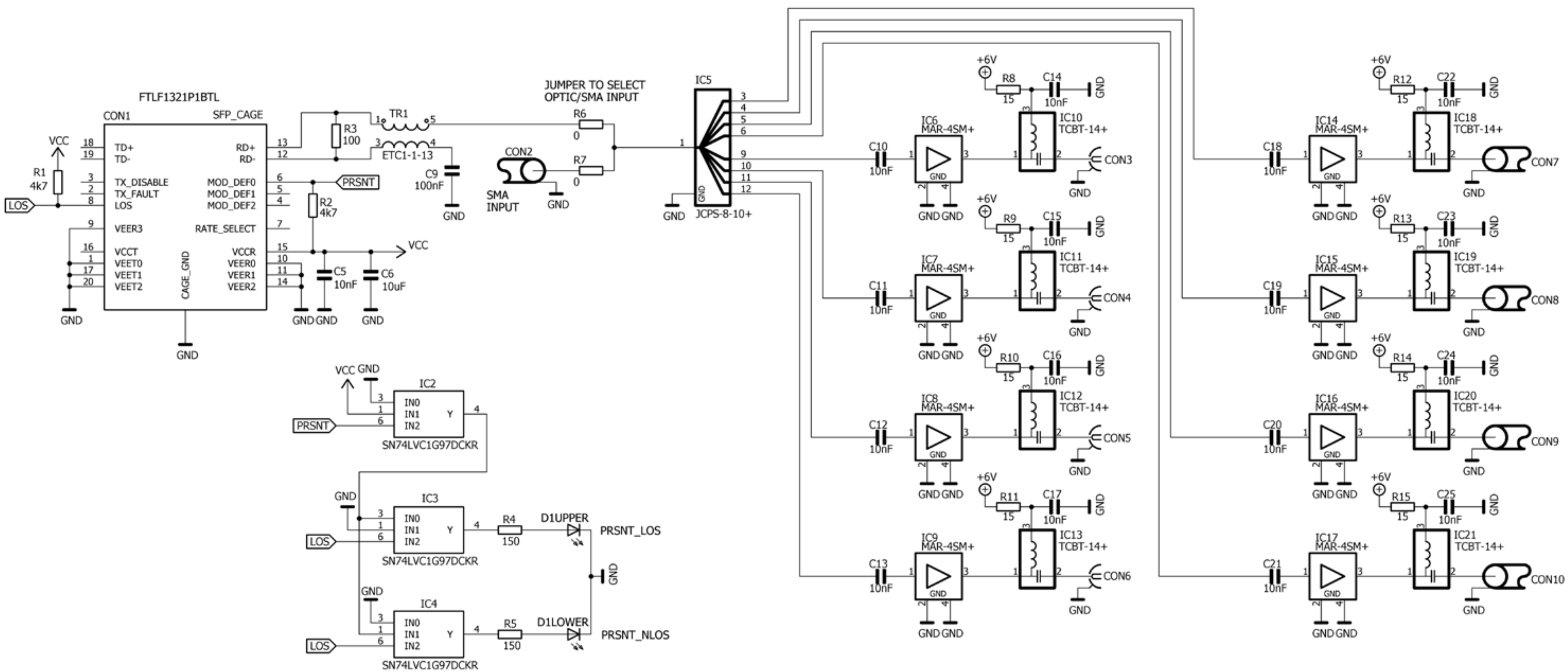
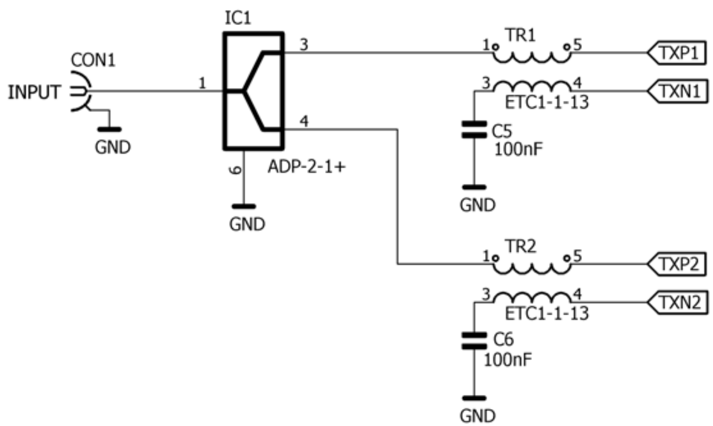
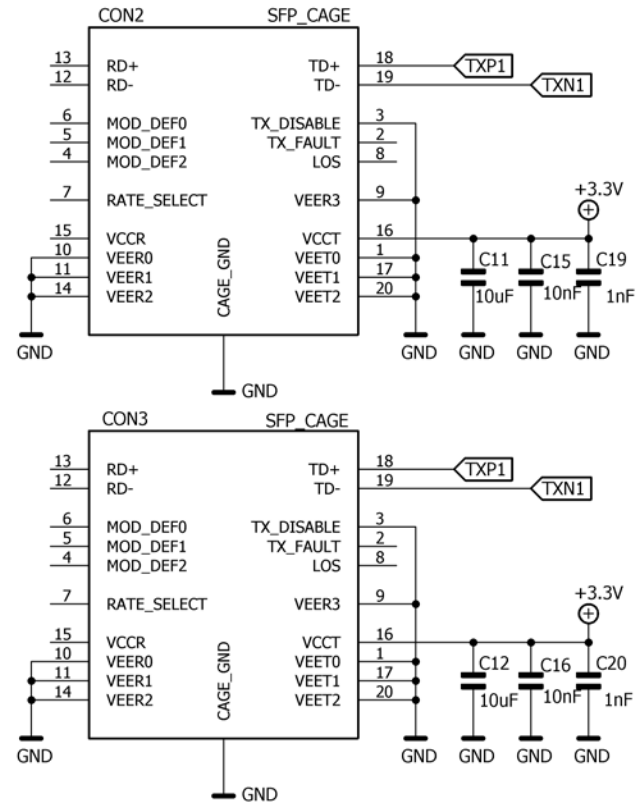
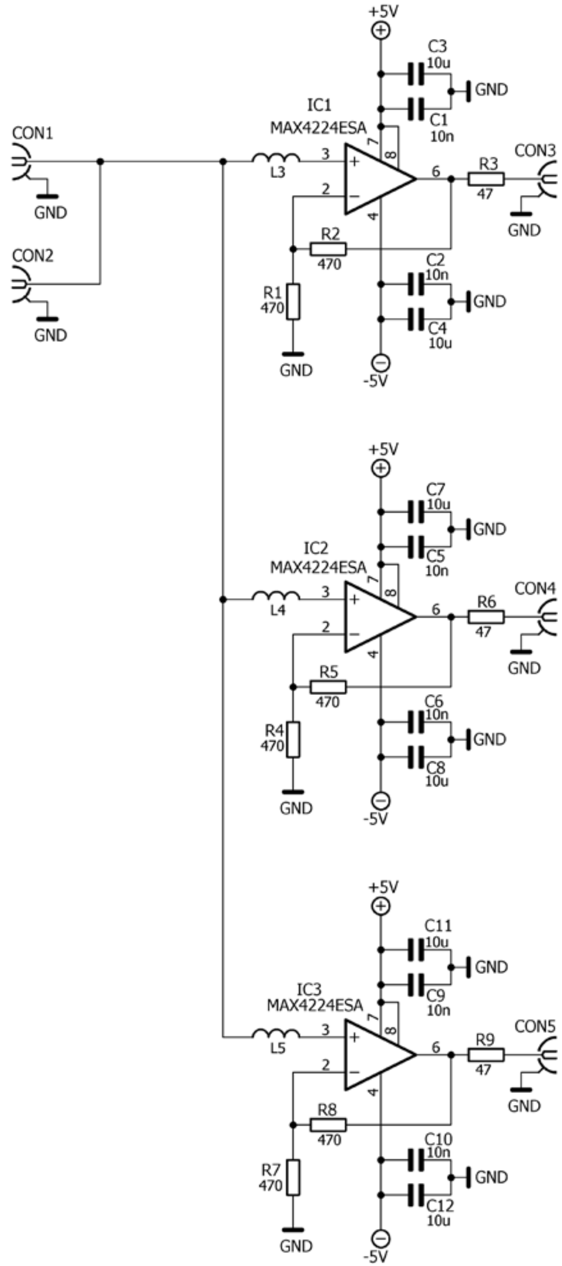
Thank you for your attention


GND
+2.5V
8x PT1000 assembled on the thermostat heater boards (AED-00242-V1)
PTA
PTB
+5V
C6
100n
GND
IC6
AD621ARZ
RG
REF
TEMP
C7
-5V
R26
R27
R28
R29
R22
R23
R24
R25
1k
+2.5V
R21
R20
R8
500
R17
R18
Temperature setpoint
IC7
AD621ARZ
C8
C9
SET
Measuring points
TP1 of setpoint temperature, connected
TP2 to the front panel of controller
200k
R6
P - gain
R7
I - gain
C2
IC1
AD623ARZ
C1
C3
IC2
AD623ARZ
C4
P
R3
10k
Sum of P and I
R4
IC3B
TL072CD
R16
330
CTRL
D1
PMLL4148L
Integrator
22u
C15
C14
C5
R5
100k
I
R1
330k
IC3A
TL072CD
R2
C12
C13


FTLF1321P1BTL
CON1
SFP_CAGE
VCC
R1
4k7
LOS
TD+
TD-
TX_DISABLE
TX_FAULT
LOS
VEER3
VCCT
VEET0
VEET1
VEET2
CAGE_GND
RD+
RD-
MOD_DEF0
MOD_DEF1
MOD_DEF2
RATE_SELECT
VCCR
VEER0
VEER1
VEER2
GND
R3
100
R2
4k7
PRSNT
C5
10nF
C6
10uF
TR1
ETC1-1-13
C9
100nF
JUMPER TO SELECT
OPTIC/SMA INPUT
R6
0
R7
0
CON2
SMA
INPUT
IC5
JCPS-8-10+
IC6
MAR-4SM+
IC7
MAR-4SM+
IC8
MAR-4SM+
IC9
MAR-4SM+
IC10
TCBT-14+
IC11
TCBT-14+
IC12
TCBT-14+
IC13
TCBT-14+
IC14
MAR-4SM+
IC15
MAR-4SM+
IC16
MAR-4SM+
IC17
MAR-4SM+
IC18
TCBT-14+
IC19
TCBT-14+
IC20
TCBT-14+
IC21
TCBT-14+
+6V
R8 15
R9 15
R10 15
R11 15
R12 15
R13 15
R14 15
R15 15
C10 10nF
C11 10nF
C12 10nF
C13 10nF
C14 10nF
C15 10nF
C16 10nF
C17 10nF
C18 10nF
C19 10nF
C20 10nF
C21 10nF
C22 10nF
C23 10nF
C24 10nF
C25 10nF
CON3
CON4
CON5
CON6
CON7
CON8
CON9
CON10
IC2
IC3
IC4
IN0
IN1
IN2
Y
SN74LVC1G97DCKR
R4
150
R5
150
D1UPPER
D1LOWER
PRSNT_LOS
PRSNT_NLOS


CON1
INPUT
GND
IC1
ADP-2-1+
TR1
ETC1-1-13
TXP1
TXN1
C5
100nF
TR2
ETC1-1-13
TXP2
TXN2
C6
100nF


CON2
SFP_CAGE
RD+
RD-
MOD_DEF0
MOD_DEF1
MOD_DEF2
RATE_SELECT
VCCR
VEER0
VEER1
VEER2
CAGE_GND
TD+
TD-
TX_DISABLE
TX_FAULT
LOS
VEER3
VCCT
VEET0
VEET1
VEET2
TXP1
TXN1
+3.3V
C11
10uF
C15
10nF
C19
1nF
GND
CON3
SFP_CAGE
C12
10uF
C16
10nF
C20
1nF


+5V
C3
10u
GND
C1
10n
IC1
MAX4224ESA
CON1
L3
R3
47
CON3
GND
GND
R2
470
CON2
C2
10n
R1
470
GND
GND
C4
10u
GND
-5V
+5V
C7
10u
GND
C5
10n
IC2
MAX4224ESA
L4
R6
47
CON4
GND
R5
470
C6
10n
R4
470
GND
C8
10u
GND
-5V
+5V
C11
10u
GND
C9
10n
IC3
MAX4224ESA
L5
R9
47
CON5
GND
R8
470
C10
10n
R7
470
GND
C12
10u
GND
-5V