Design Status of the **CERN-SRAM** macrocell

IBM 0.25 μm User Group Meeting

Imperial College, London

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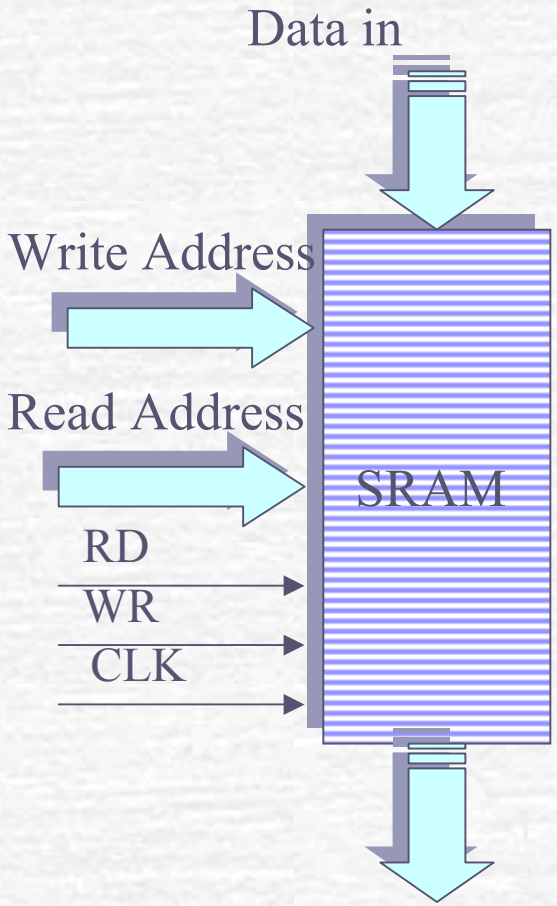
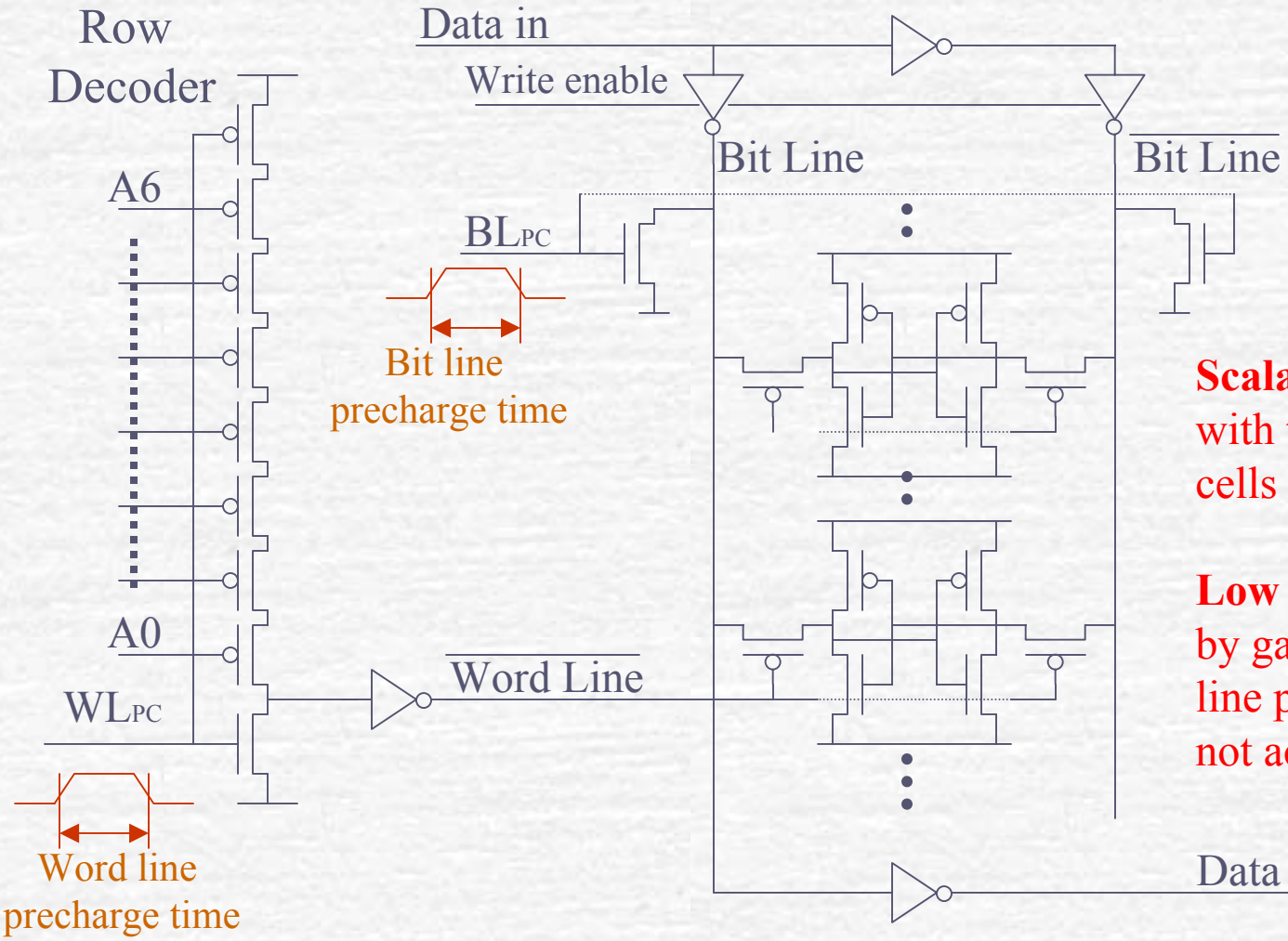
EP/CME-PS

CERN-SRAM specifications

- Scalable Design
  - Configurable Bit organization (n x 9-bit).
  - Configurable Memory Size.
- Synchronous Dual-Port Operation
  - Allowing Read/Write operations on the same clock cycle.
  - Typical Operating Frequency: 40 Mhz.
- Low Power Design
  - Full Static Operation.
  - Two stage hierarchical word decoding.
- Radiation Tolerant Design



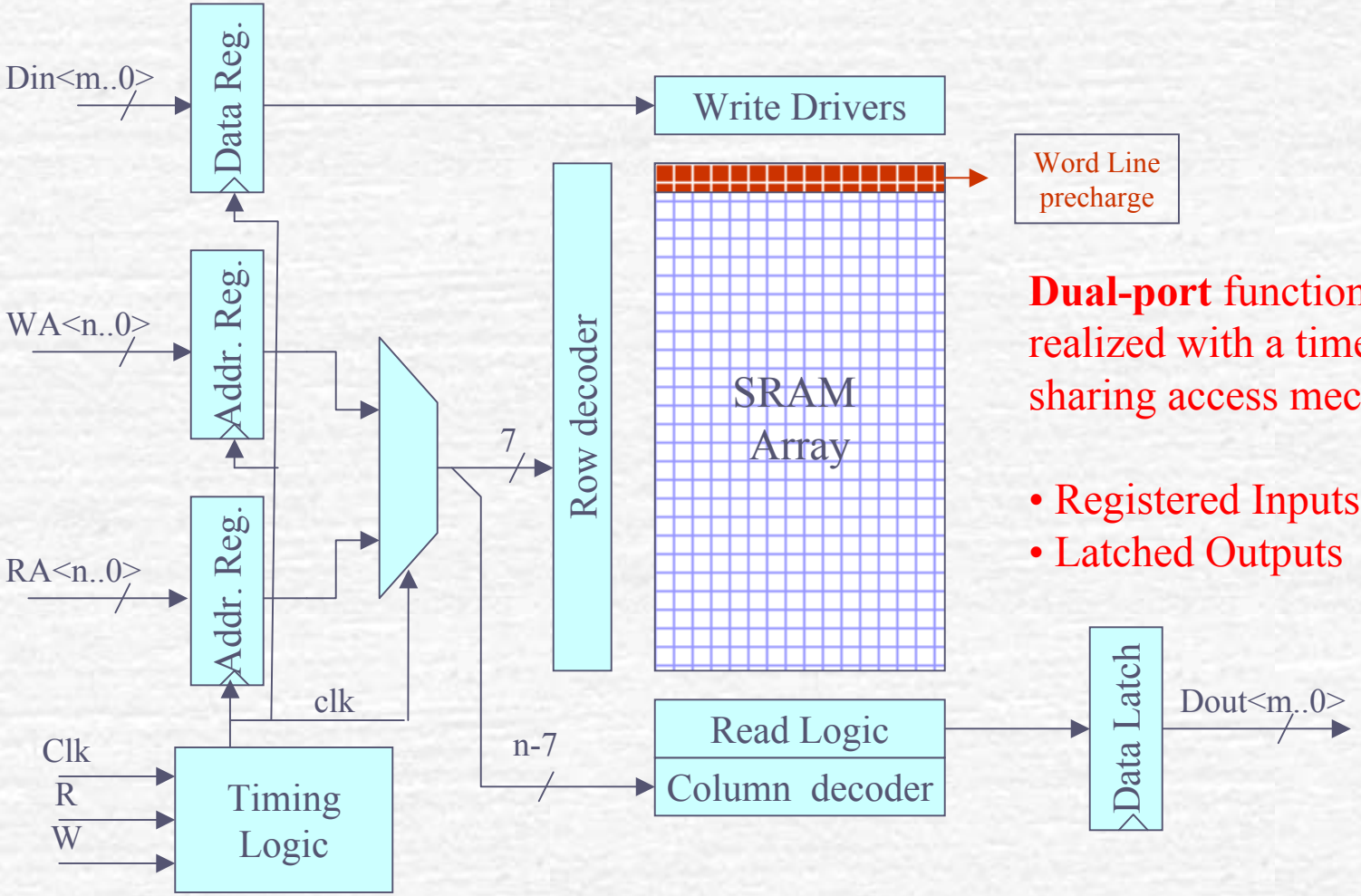
SRAM Design in 0.25μ



Scalability is accomplised with the use of replica row cells and wordlines.

Low Power is enhanced by gating bit-line & word-line precharge cycles when not accessing the memory.

Dual Port SRAM
block diagram

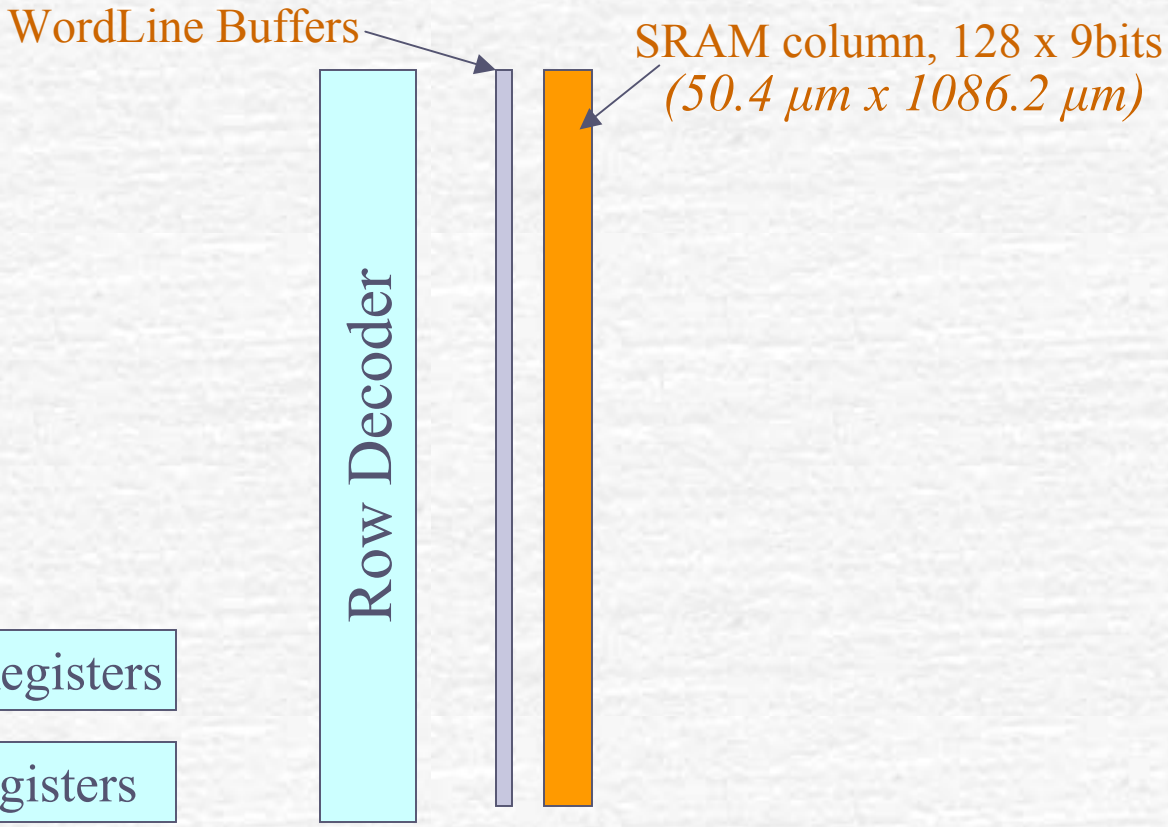


Dual-port functionality is realized with a time sharing access mechanism.

- Registered Inputs
- Latched Outputs

Timing of the SRAM Interface

Basic Layout Blocks



Input Data Registers

Address Registers

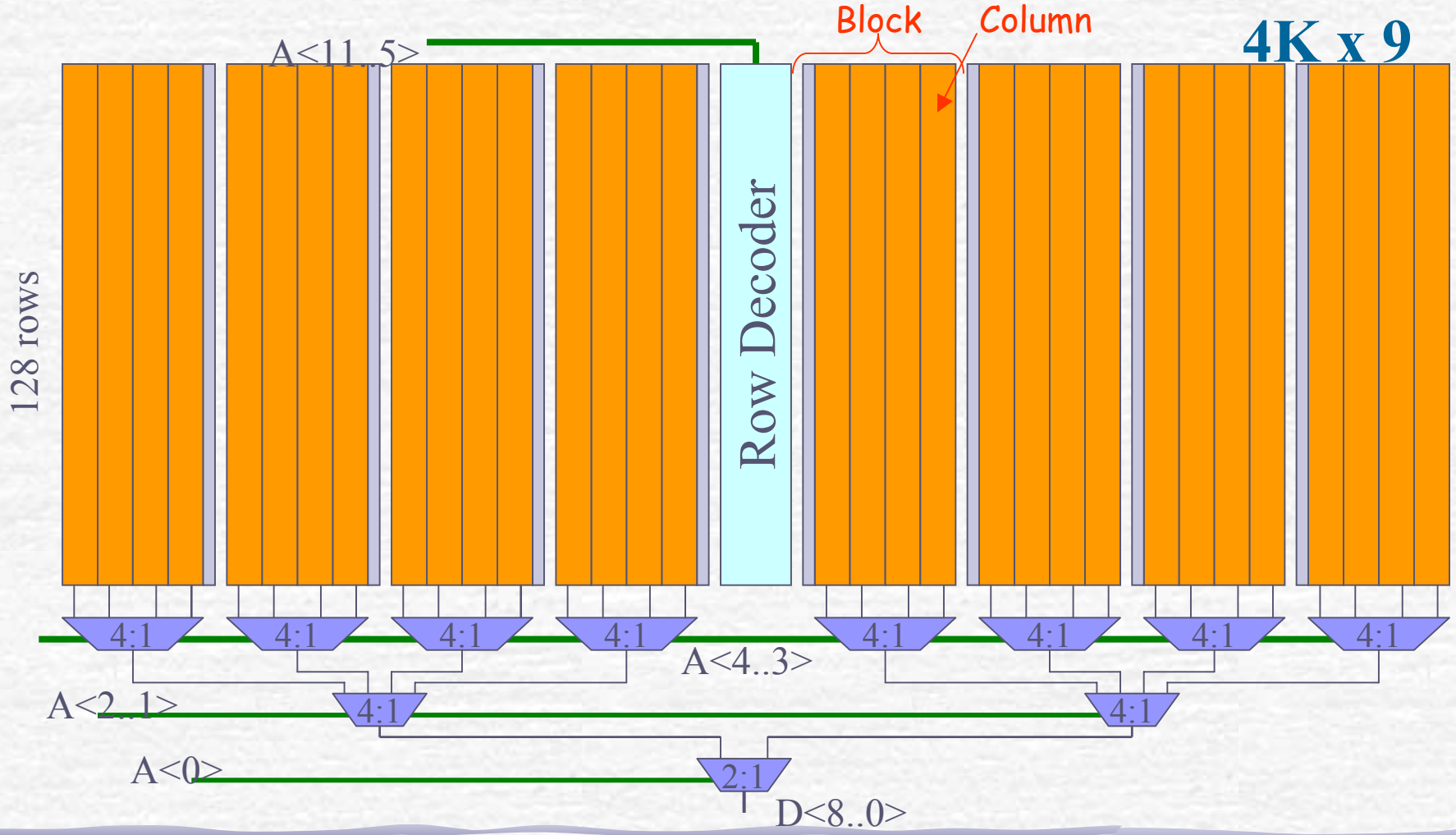
Timing logic

Column Decoder

Output Data Mux

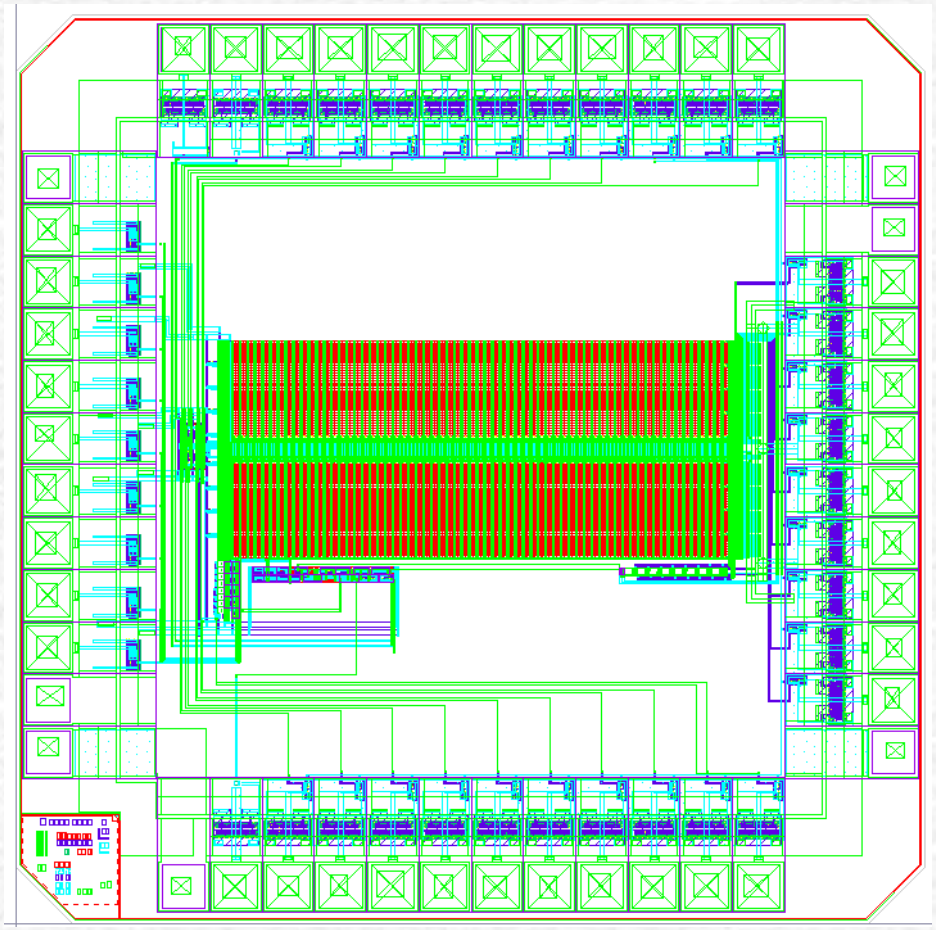
Output Data Latches

Modular SRAM design.



Submitted SRAM Chips

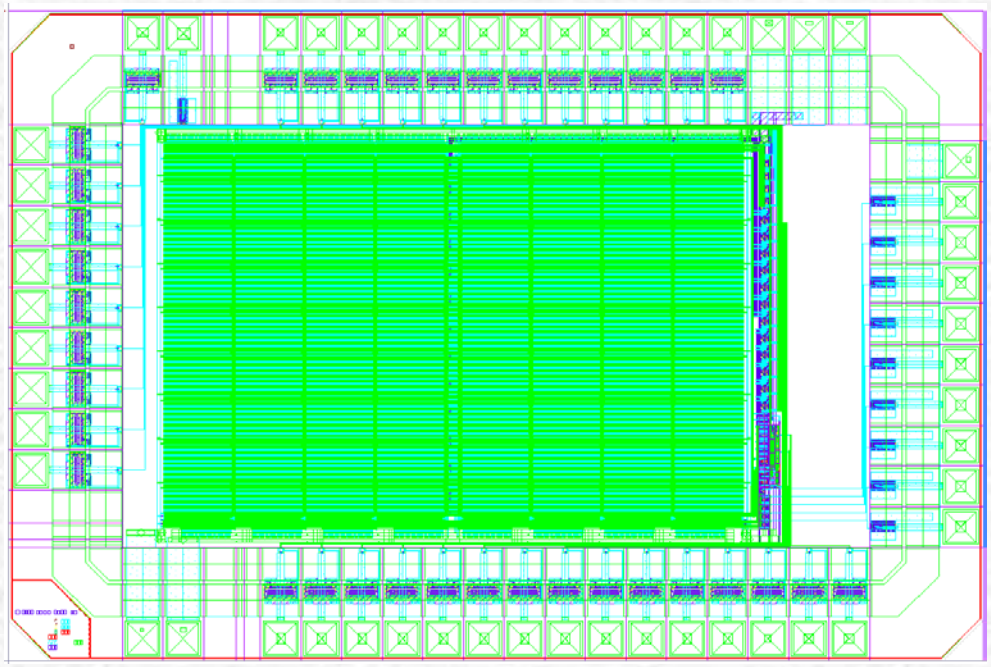
- 1st Prototype (CERN MPW 4)
- Configuration: 1Kx9 bit
- Size: ~560μm x 1,300μm
- Area: ~0.73mm²
- Submitted: Oct. 2000.
- Chip Received: Feb 2001
- Tested: Apr. 2001
- Status: O.K.



Design: CERN_SRAM_1K
Designer: Kloukinas Kostas
EP/CME-PS

Submitted SRAM Chips

- 2nd Prototype (CERN MPW 5)
- Configuration: 4Kx9 bit
- Size: ~1,850μm x 1,300μm
- Area: ~2.4mm²
- Submitted: May 2001
- Chip Received: Aug. 2001
- Tested: Oct. 2001
- Status: O.K.



Design: CERN_SRAM_4K
Designer: Kloukinas Kostas
EP/CME-PS

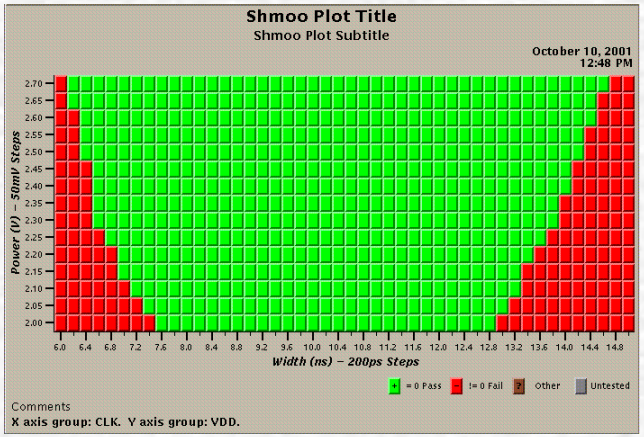
CERN SRAM test results

Test chip: 4Kx9bit

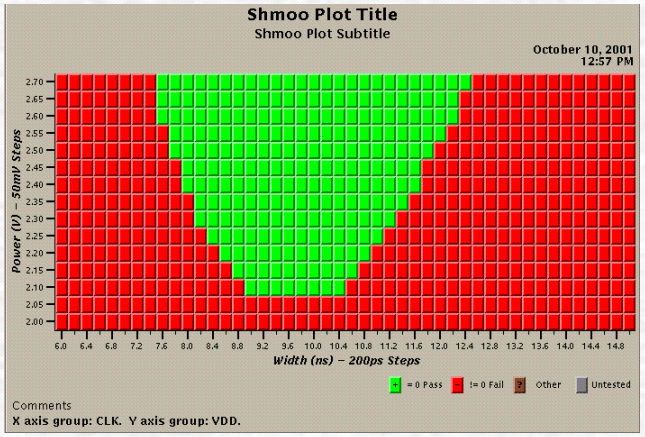
- Functional tests
  - Max operating frequency:
    - Read only operations per clock cycle : 75MHz @ 2.5V
    - Read/Write operations per clock cycle : 60MHz @ 2.5V
  - Read access time: 7.0ns @ 2.5V
  - Power dissipation:
    - 15μW / MHz @ 2.5V for R/W operations within the same clock cycle (0.60mW @ 40MHz).
  - Tests for process variations:
    - Differences in the access time < 1ns for: -3σ, –1.5σ, typ, +1.5σ, +3σ

Clock Duty Cycle Tests

50MHz Read per cycle

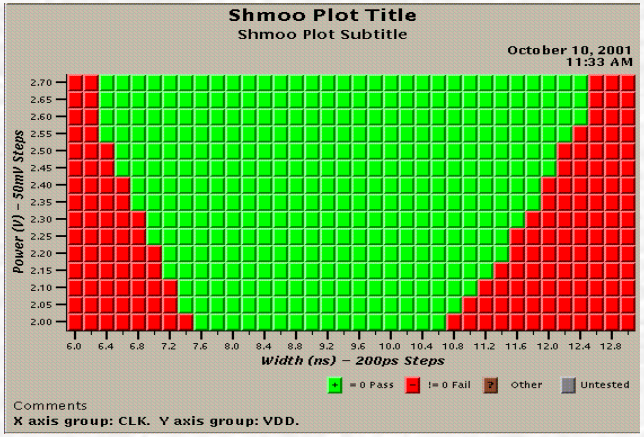


Read/Write per cycle

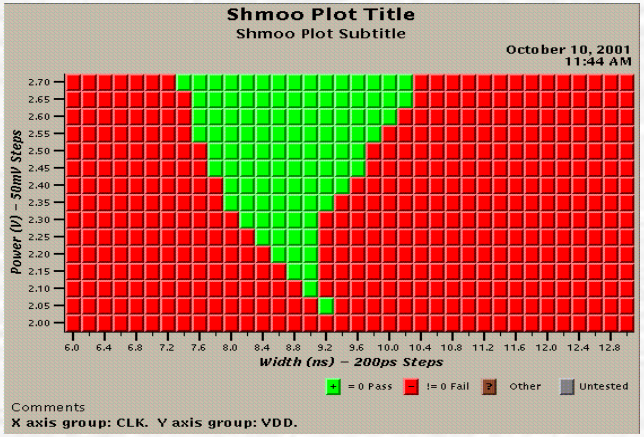


Test chip: 4Kx9bit

55MHz Read per cycle



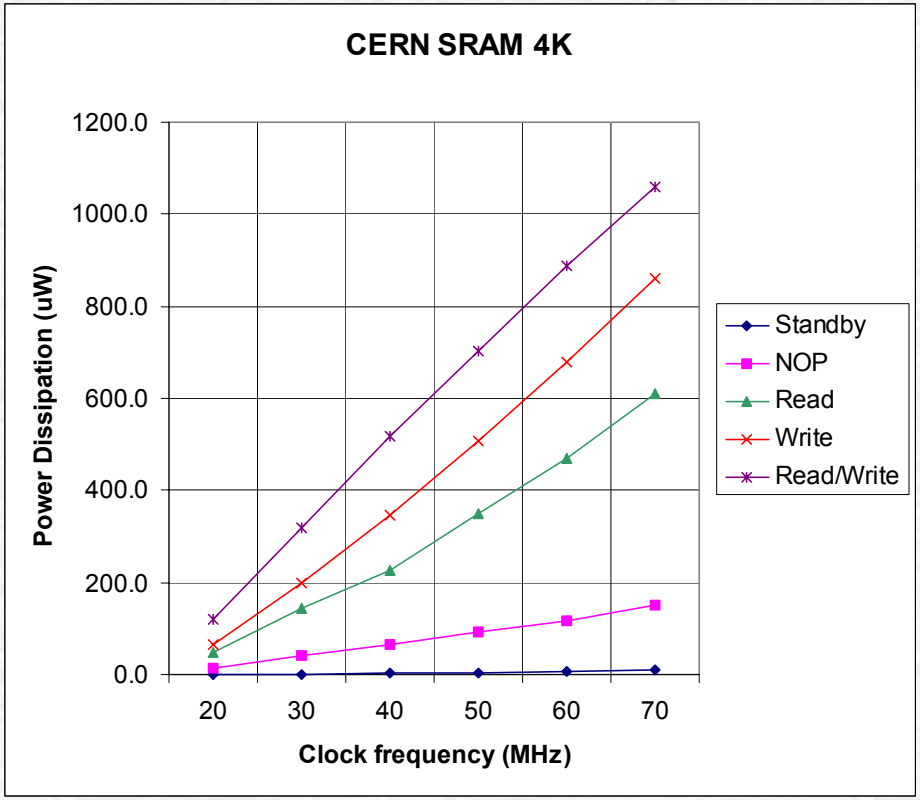
Read/Write per cycle



Duty Cycle variations

50 MHz	50% ± 20%
55 MHz	50% ± 10%
60 MHz	50% ± 5%

Power dissipation



Test chip: 4Kx9bit

Operation	Power (uW/MHz)
Standby	0.10
NOP	1.90
Read	7.40
Write	10.60
Read/Write	14.05

Test Conditions

Operation	Description	Pattern File
Standby	No operation, addr. & data in to highz	nop1.set
NOP	No operation, addr. & data changing in every c	nop2.set
Read	checkerboard data pattern	SRAM_0.set
Write	checkerboard data pattern	SRAM_0.set
Read/Write	checkerboard data pattern	SRAM_1.set

Irradiation Tests

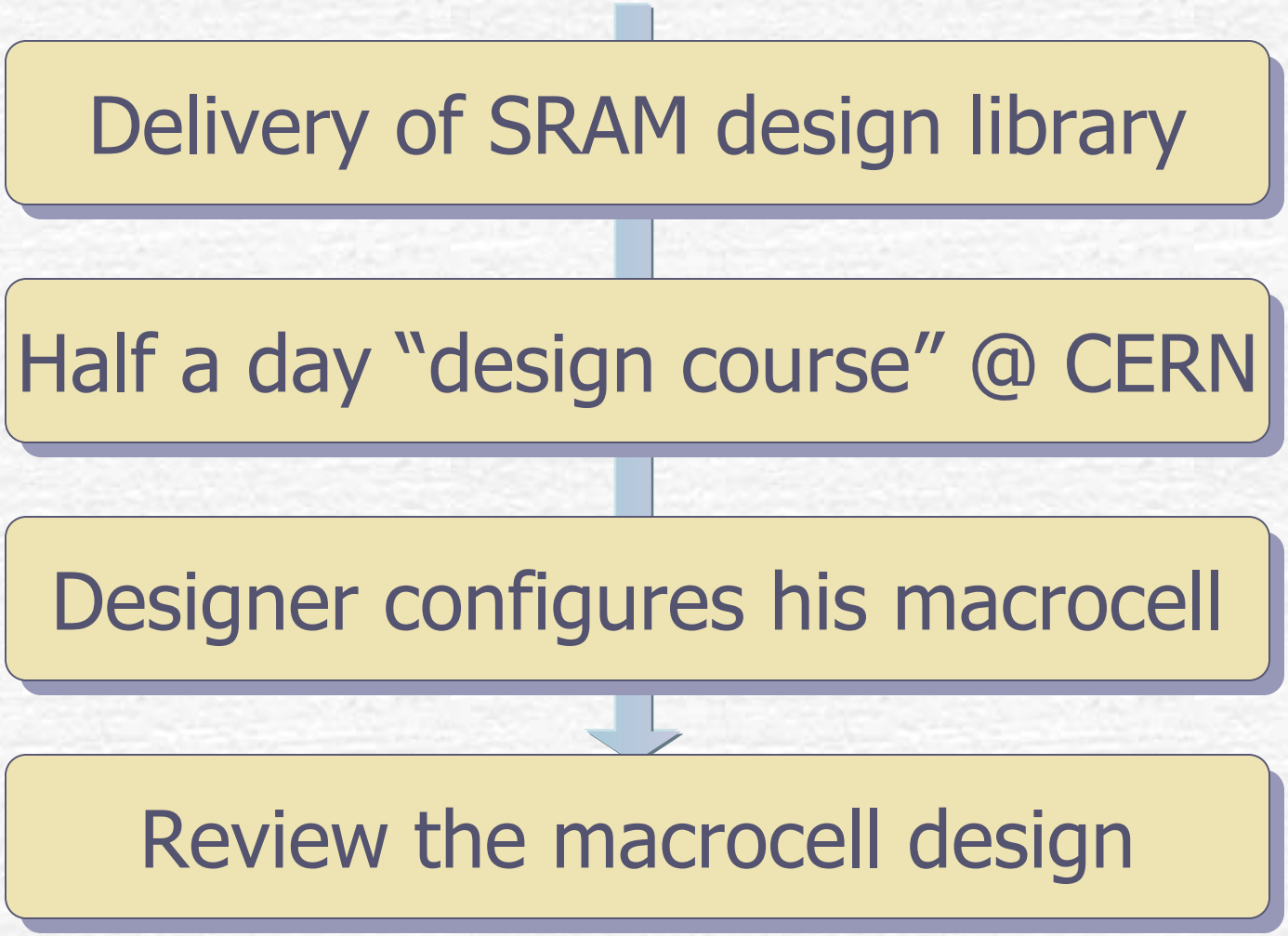
Test chip: 4Kx9bit

- Ionizing Total Dose: up to 10MRad
  - No increase in power dissipation.
  - No measurable degradation in performance.
- Single Event Upset:
  - under preparation
    (in collaboration with CERN EP/MIC group)

CERN SRAM popularity !

- ATLAS SCAC chip
  - Memory configuration: 128 x 18bit
  - Detector: ATLAS tracker
  - Lab: NEVIS Labs
  - Designer: Stephan Boettcher
  - Status: Tested O.K.
- ATLAS DTMROC chip
  - Memory configuration: 128 x 153 bits
  - Detector: ATLAS TRT
  - Lab: CERN
  - Designer: Robert Szczygiel
  - Status: Tested O.K.
- CMS K chip
  - Memory configuration: 2K x 18 bits
  - Detector: CMS Preshower
  - Lab: CERN
  - Designer: Kostas Kloukinas
  - Status: work in progress
- ATLAS MCC chip
  - Memory configuration: 128 x 27bit
  - Detector: ATLAS PIXEL
  - Lab: INFN Genova
  - Designer: Roberto Beccherle
  - Status: Tested O.K.
- ALICE AMBRA chip
  - Memory configuration: 16K X 9 bits
  - Detector: ALICE Silicon Drift Det.
  - Lab: INFN Torino
  - Designer: Gianni Mazza
  - Status: Submitted
- ALICE CARLOS chip
  - Memory configuration: 256 X 9 bits
  - Detector: ALICE Silicon Drift Det.
  - Lab: INFN Bologna
  - Designer: Alessandro Gabrielli
  - Status: work in progress

Design Support



Conclusions

- Design Status
  - Design meets specifications.
  - Macrocell has been successfully used in a number of ASIC designs.
- Future Plans
  - None. No further development is foreseen.
- Design Support
  - Contact Person: Kostas.Kloukinas@CERN.ch
- Information on the Web
  - http://home.cern.ch/kkloukin